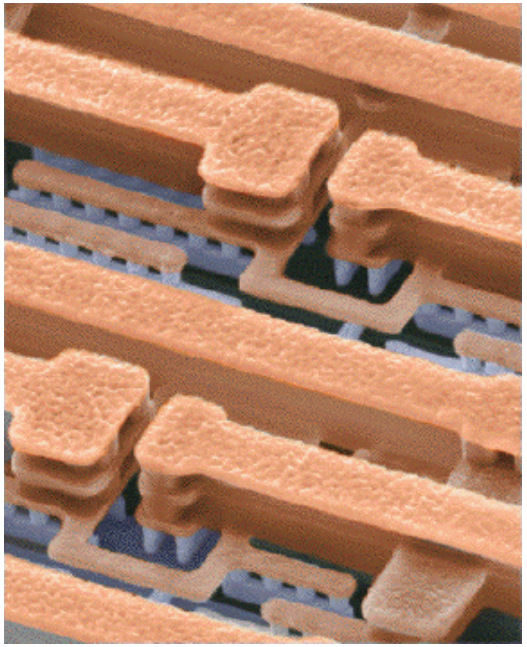
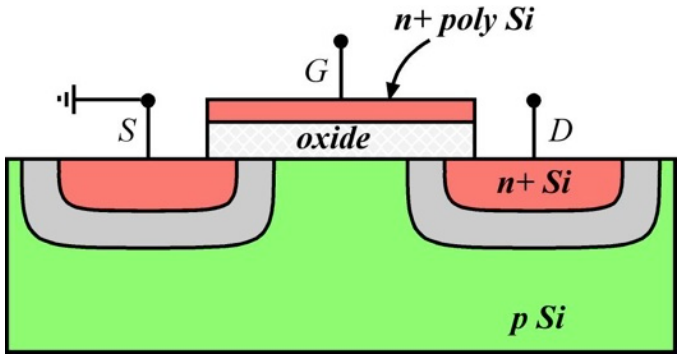
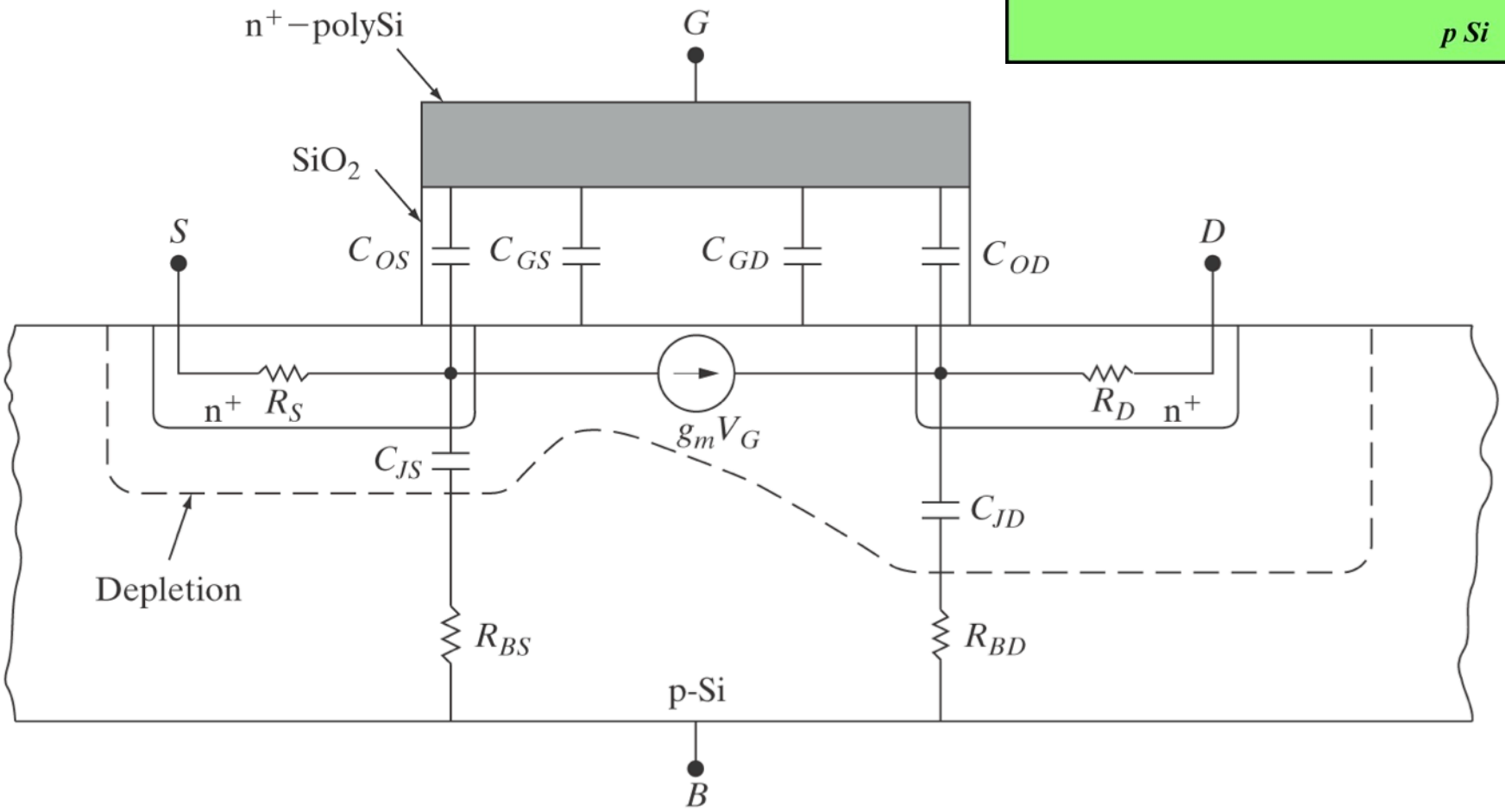
(no chapter sections) – Advanced MOS Topics



- Equivalent Circuit
- Power MOSFETs (amplifiers)
- Semiconductor memory (DRAM, Flash)
- Fabrication Advances
- Next generation architectures (FinFETs?)

- Just so you are aware of it, Fig. 6-39 provides the equivalent circuit for a MOSFET (assumes is above threshold).

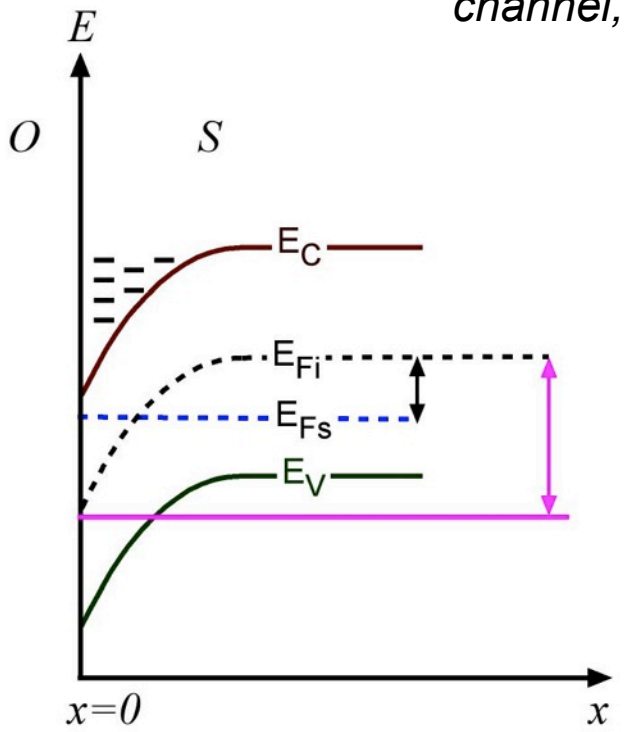


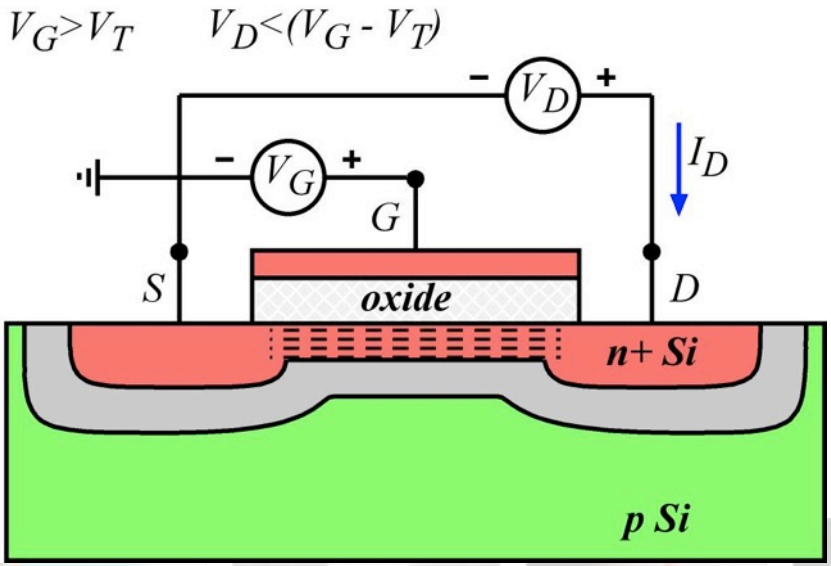


- MOSFETS are increasingly used for power switching applications, but our design we would not use for power switching… why not?

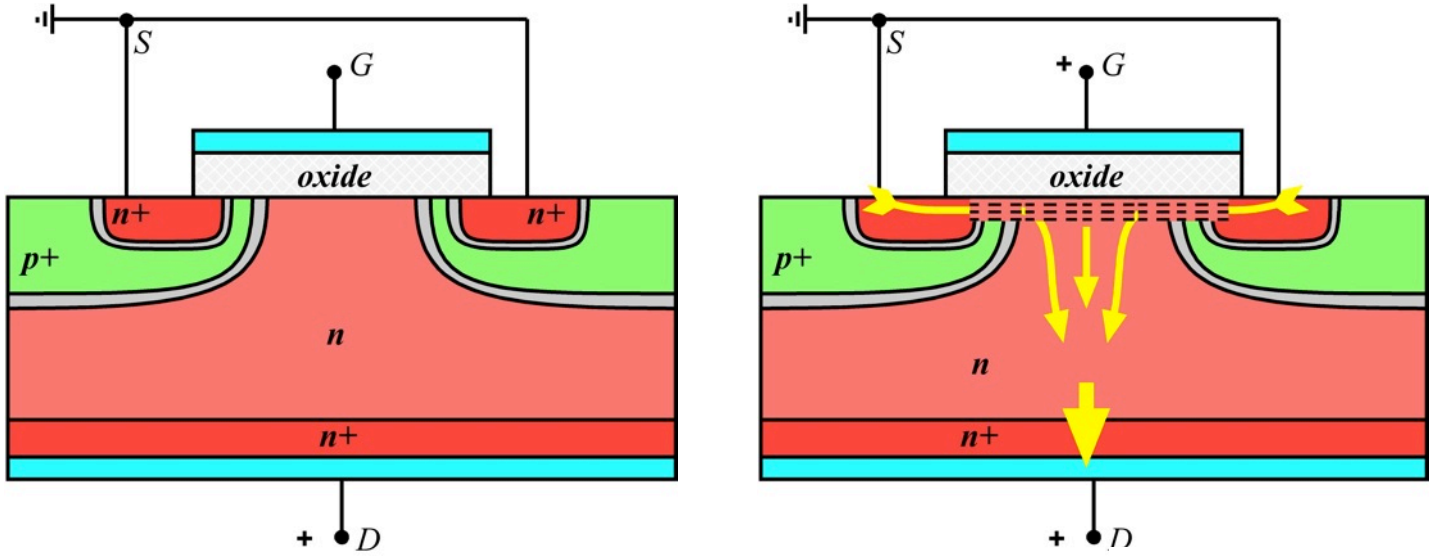
W_m ~ 100's nm and bulk of current is near surface (1's to 10's nm) … so what does our resistor look like?

If we drive a very high value of current through the channel, what will happen?





- For power switching applications, you need to reduce the channel length and spread out the current VERY quickly! (example, Hybrid electric cars)

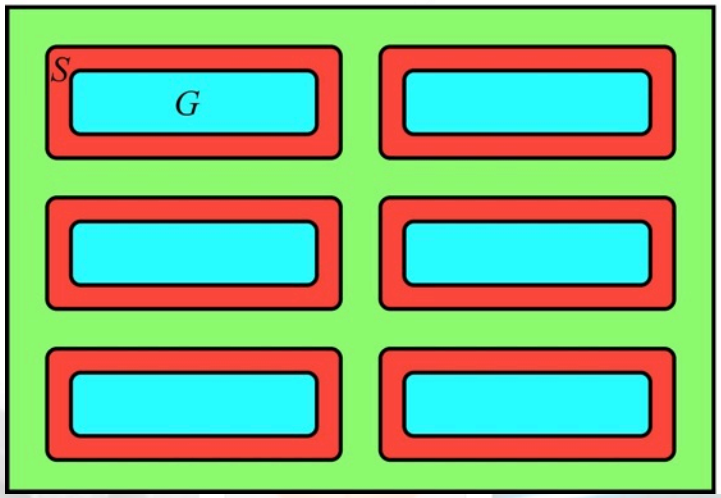


High current (10's A) by running up to 1000's in parallel on same chip…

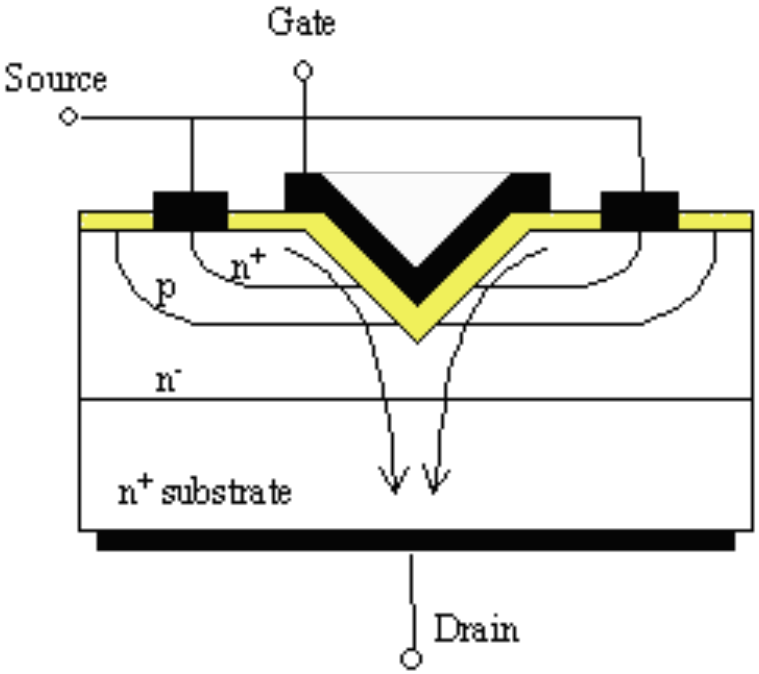
- For power switching, power MOSFETS have replaced BJTs

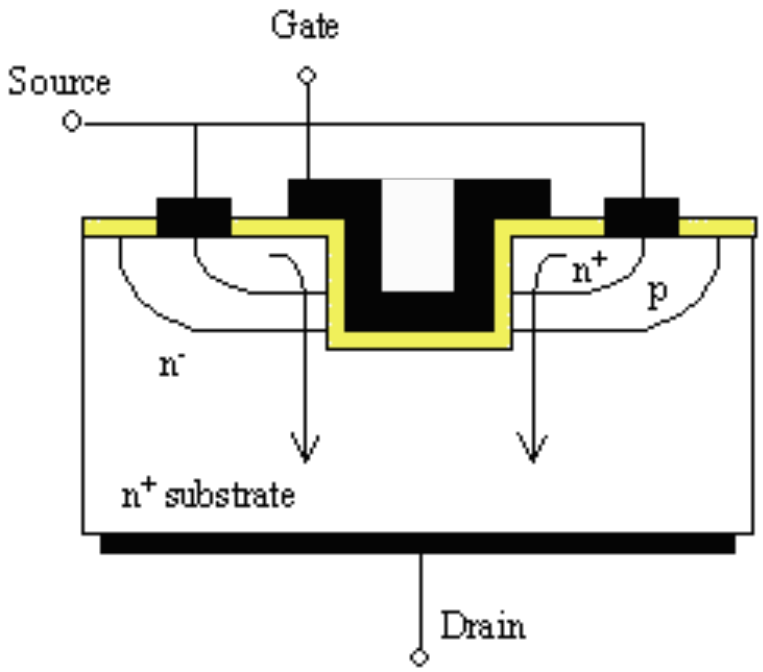
- The BJT is still great in discrete circuit design (many ways to run it as you learn in Electronics, very versatile)…. Also BJT's dominate in radio-frequency circuits for wireless communications (10's to 100's of MHz).

why rounded corners?



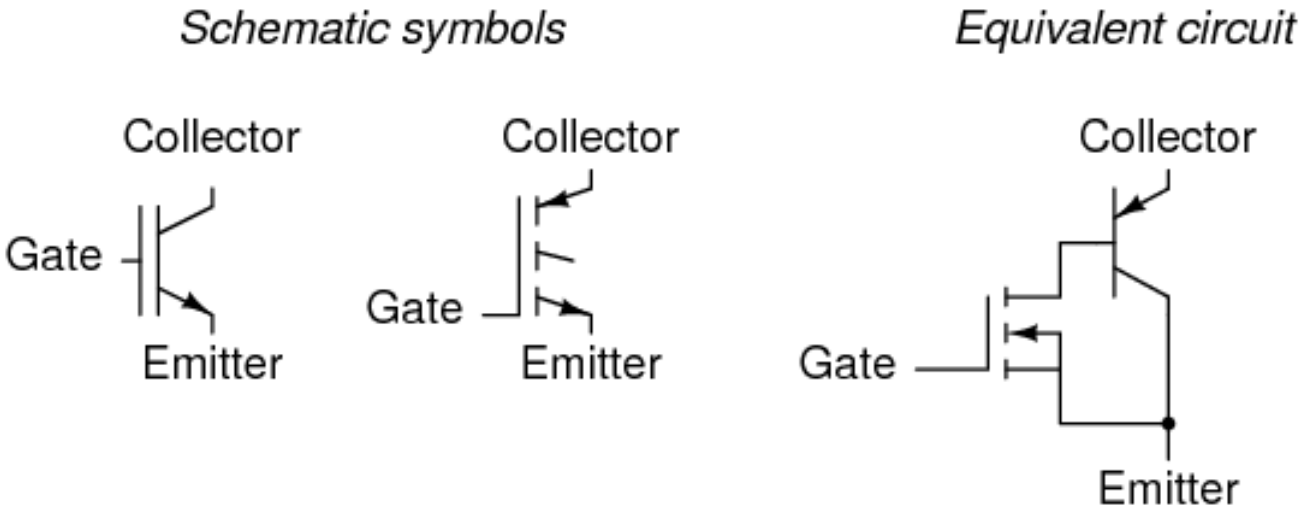
- Some alternate designs… (ecee.colorado.edu/~bart/book/book/chapter7/ch7_8.htm)





- Until 70's/80's BJT was device of choice in the design of discrete and integrated circuits
- Today CMOS dominant in integrated circuits
- BJT is the choice for demanding analog circuits, both integrated and discrete. Excellent in very-high-frequency and higher-power applications, such as RF circuits for wireless systems.
- The bipolar transistors can be combined with MOSFET's in an integrated circuit by using a BiCMOS process. Why combine them???
- Careful, lots of names, even I am not sure sometimes if is BiCMOS or something else…

Insulated-Gate Bipolar Transistor (IGBT)
(N-channel)



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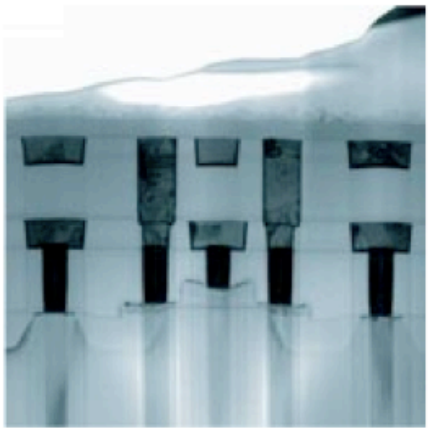
Wireless Semiconductor Technologies

Our engineers continue to refine architectures and drive further integration to deliver exactly what the wireless industry is looking for: improved performance that results in fewer dropped calls and long battery life at lower costs. Read further to find out more about our broad portfolio of wireless semiconductor technologies.



Microscopic view of SiGe:C RF BiCMOS

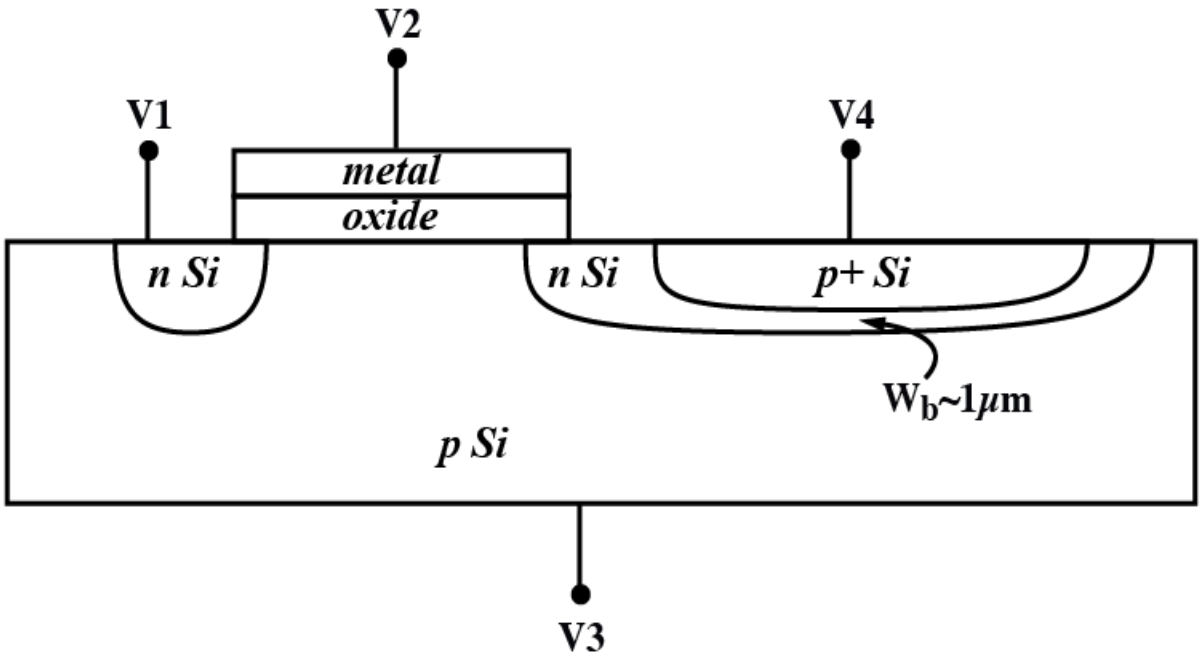
RF Leadership
The Silicon Germanium:Carbon (SiGe:C) modules of our 0.18-micron and 0.35-micron radio frequency bipolar complementary metal-oxide semiconductor (RF BiCMOS) processes require the addition of only one masking step into these proven mainstream processes. Additionally, these BiCMOS processes integrate a wide variety of high-quality active and passive devices on-chip, including copper inductors and transformers, to optimize system performance and to help significantly reduce the number of external components. The SiGe:C process produces cost-efficient, low-power, high-performance RF BiCMOS system-on-chip (SoC) solutions.

Target applications for our RF CMOS process include wireless connectivity (Ultra-Wideband and ZigBee) as well as cellular handsets and data modems. Freescale plans to apply RF CMOS technology to the creation of single-chip radios, defined as RF plus baseband, and to improve the cost effectiveness of RF transceiver functions.

Freescale?s Indium Gallium Phosphide heterojunction bipolar transistor (InGaP HBT) process is a key technology used for power amplifiers and power amplifier modules. The InGaP HBT technology provides high-efficiency, high-performance, cost-effective power amplifiers that can operate with a single-voltage power supply. Freescale?s SMARTMOS? technology family couples several generations of baseline CMOS technology with analog and voltage robust enhancements. SMARTMOS technology flows integrate intelligent digital control, high-performance analog circuitry, and power-capable devices on a single chip. This wireless semiconductor technology is ideal for designing ICs that provide power management, control logic and audio circuit functions, saving valuable space and reducing the external component count in portable products.

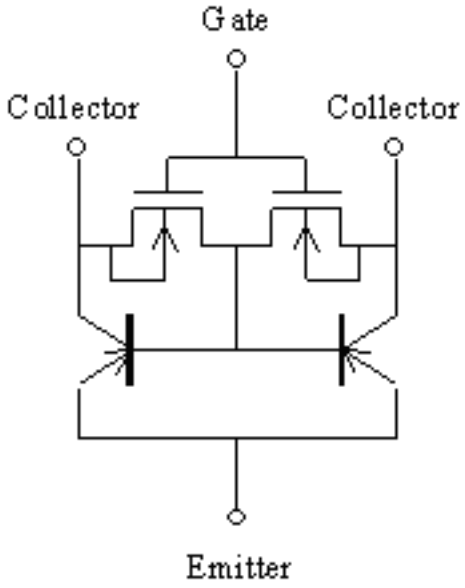
- Here is one way to do it… how would you bias it?

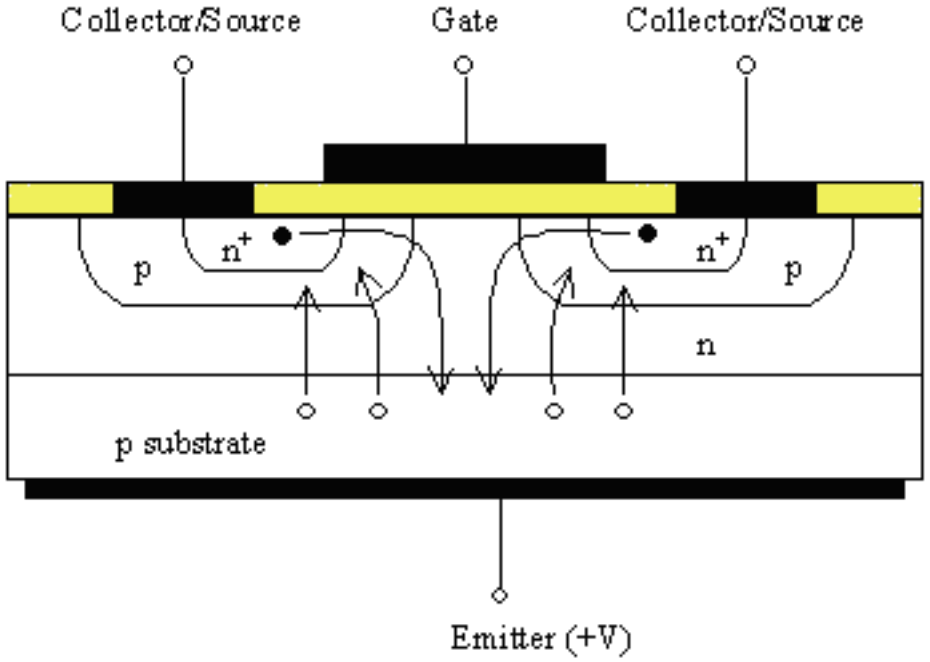
- If the device on the left side has a transconductance of $1x10^{-3}$ Siemens or (A/V) and the device on the right has an amplification factor of 100, calculate the change in current at terminal V4 when terminal V2 is changed by 1 V.



- Here is another way (http://ecee.colorado.edu/~bart/book/book/chapter7/ch7_8.htm)

Simple! The gate allows electron injection from the 'source' into the n-type base of a PNP BJT. Only need one contact for both the collector (BJT) and the source (FET).





- Take a break! Make sure you are solid on the ☆'ed items!

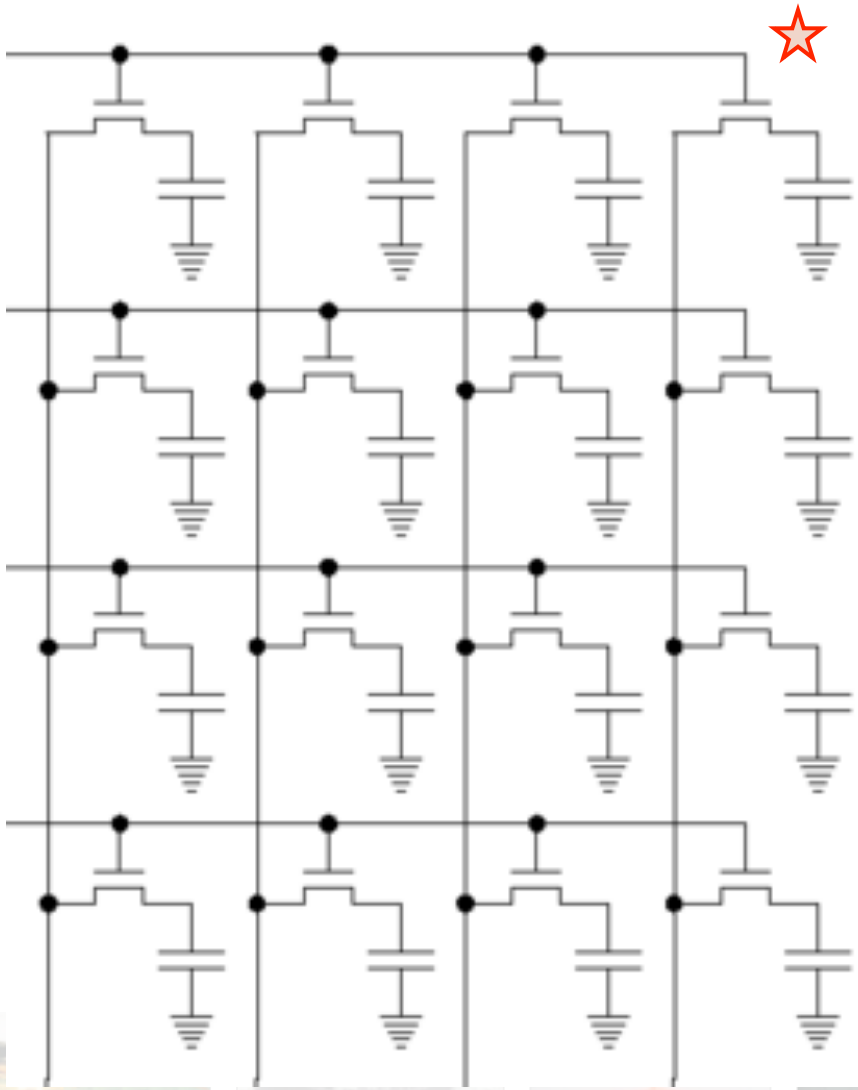
- We will examine three types of MOS-Based Memory devices: DRAM / SRAM /Flash

- First, dynamic random access memory (DRAM). Key features include:

-read or write any bit in a 1C1T cell (one MOS capacitor, one MOS transistor), is simple so can get very high density of cells per unit area!

- row electrodes turn on an entire row and columns can read or write data from single cell while that row is turned on (all other rows turned off)

-the transistor still leaks current from charged capacitor (in milliseconds) such that the DRAM must be continually refreshed, and reading data from capacitor takes time (RC)…



- So why do we have SRAM and flash?

- Second , static random access memory (SRAM). Key features include:

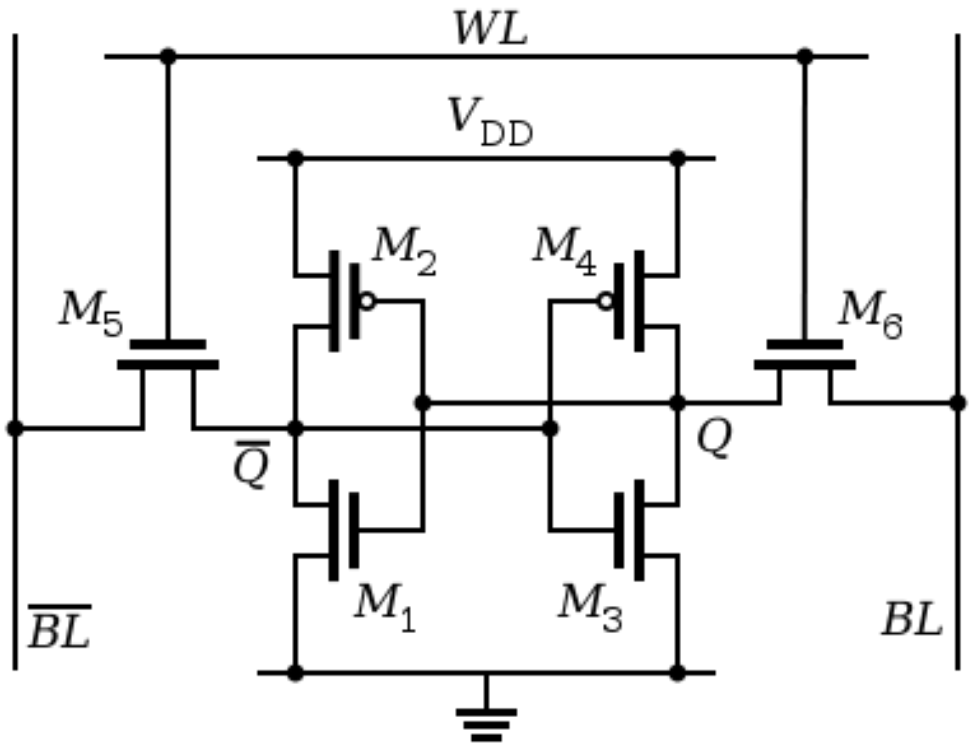
-read or write any bit in a transistor cell which consists of two cross-coupled inverters

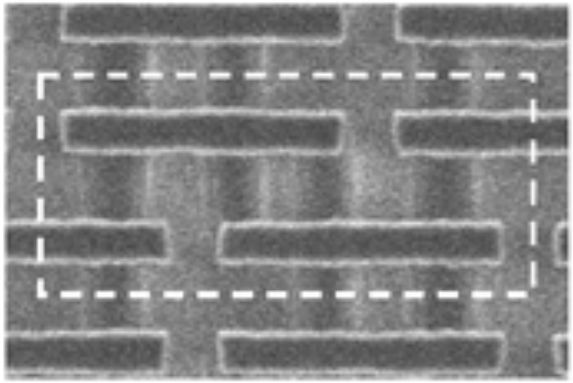
-does not need refreshed, but is always powered up, a 0 on the left inverter creates a 1 on the right inverter, and vice-versa)

- word lines allow write or read of the cell by the bit lines

-during read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell (not a weak signal from small capacitor like like DRAM)

- So why do we have DRAM, why do we have flash? Can SRAM be high density?





From Intel: SEM top-down view of the 0.346 μm² 6T-SRAM cell fabricated in the 45nm hi-k Metal-Gate CMOS technology

- Third, flash:

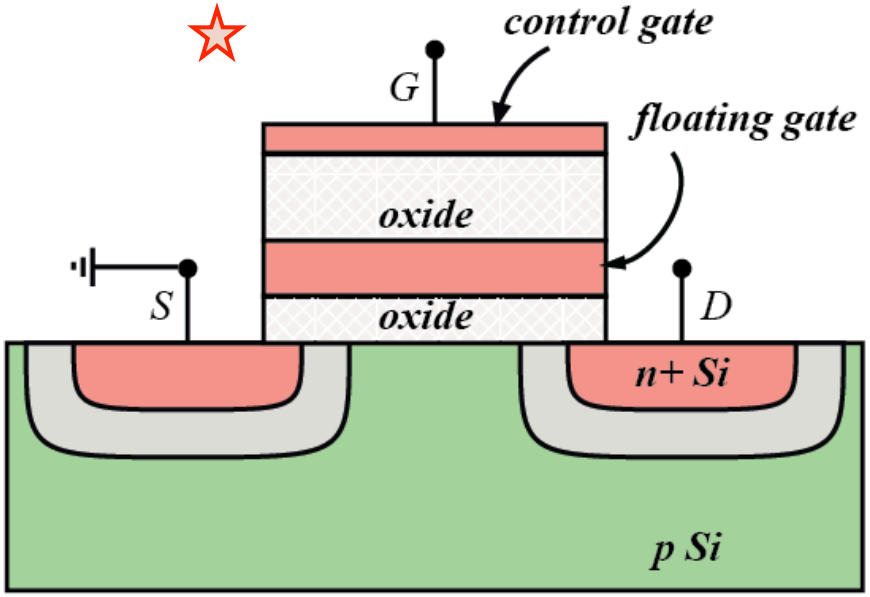
-is somewhat like DRAM except control gate can force charge from the n-channel into the floating gate (or reverse voltage to force them out), therefore storing the charge indefinitely!

- Large V_{DS} is applied to create highly energetic electrons which can get through the lower oxide to the floating gate with assistance from the control gate (how does this happen?)

-does not need refreshed, does not require power, but write time is only μs range

-also, write cycles are limited to millions before degradation of the oxide becomes too severe

- simple structure allows high density packing of cells (large memory capacity)



- So if we insert electrons into the floating gate, what does that do to V_T?
- So why do we use DRAM and SRAM for processing data? See question below…
- If you uses flash for 1 GHz processing memory (not for static storage) how long could you use use it for?

- High energy in channel helps you get through (tunnel) or over the oxide barrier…

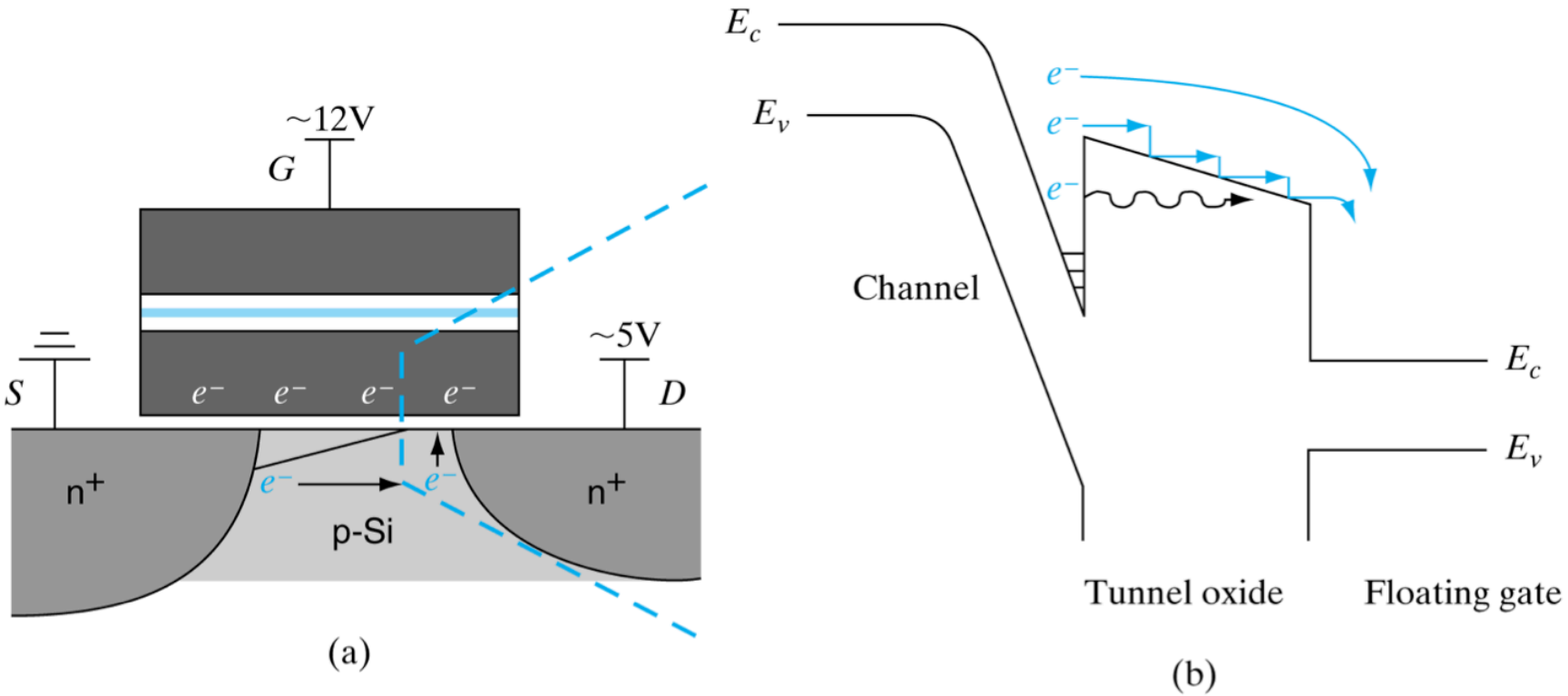


Figure 9.37

Hot carrier programming of the flash cell: (a) flash memory cell structure with typical biases required for writing into the cell. The channel of the MOSFET is pinched off in saturation; (b) band diagram along a vertical line in the middle of MOSFET channel showing hot electrons in the channel being injected across the gate oxide and getting trapped in the floating gate.

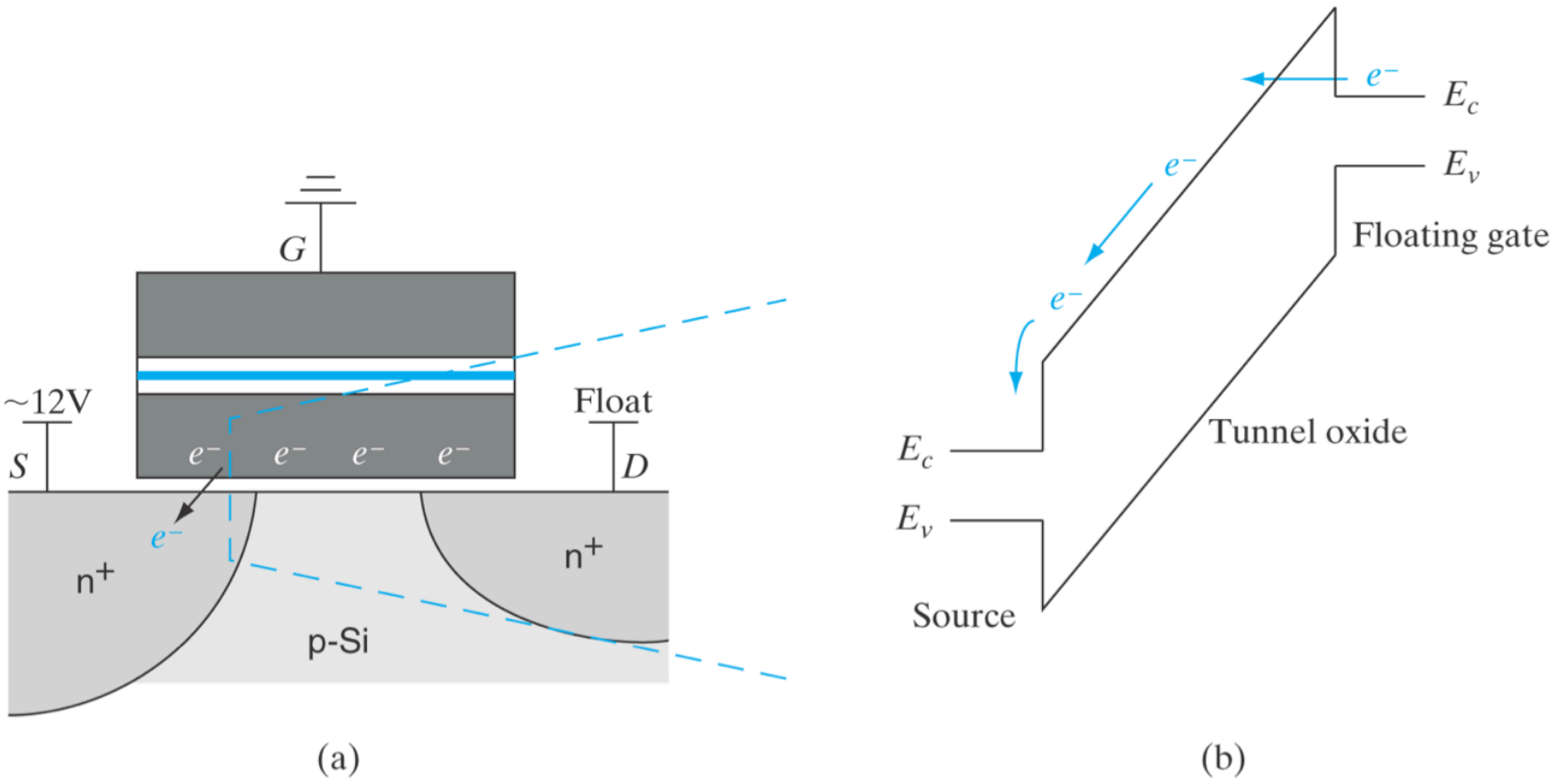


Figure 9.38

Fowler–Nordheim tunneling erasure: (a) flash memory cell structure with typical biases required for erasing the cell; (b) band diagram as a function of depth in the gate/source overlap region of the MOSFET showing quantum mechanical tunneling of carriers from the floating gate into the oxide, and subsequent drift to the source.

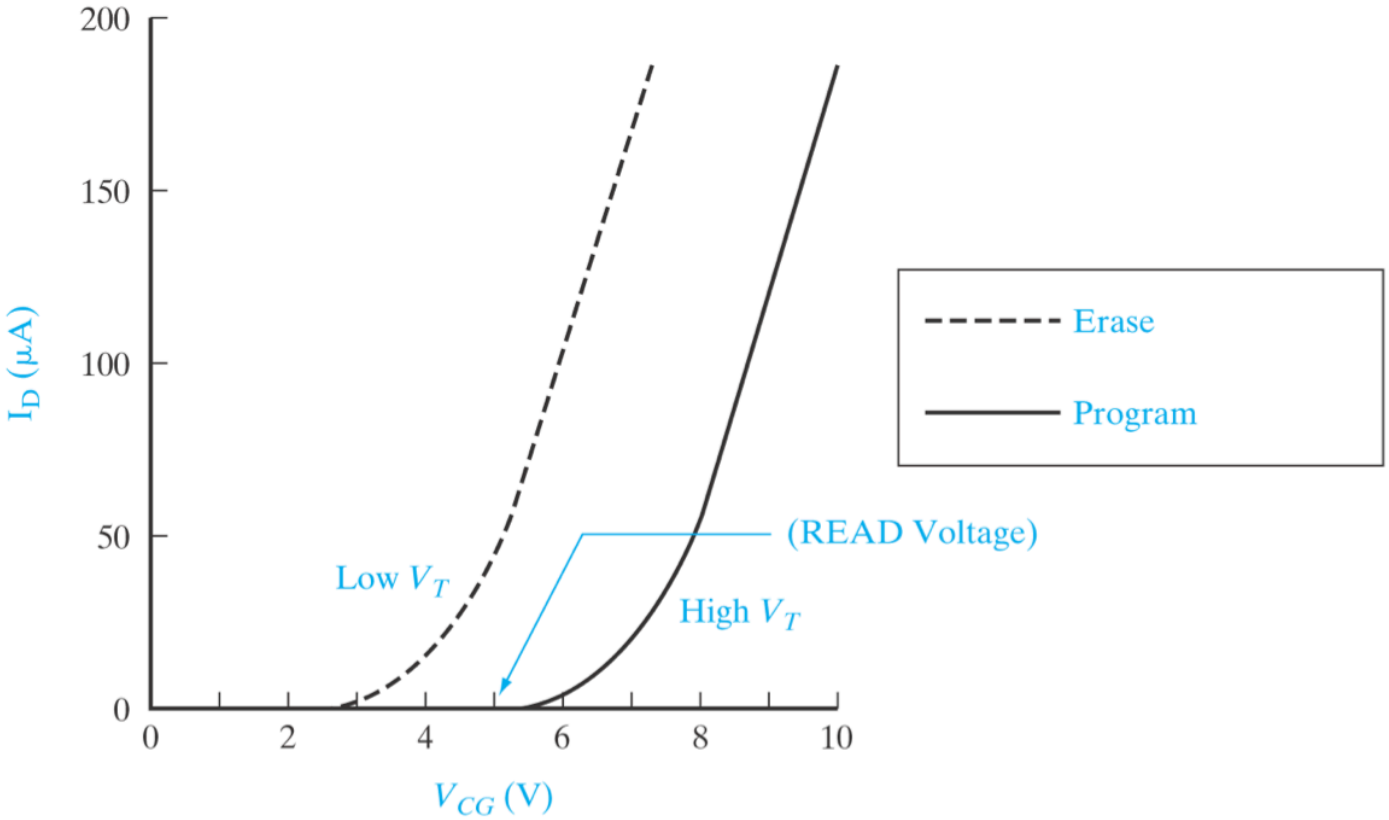
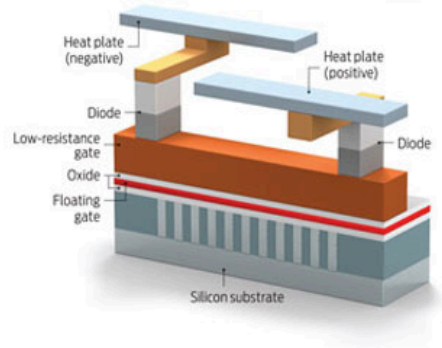


Figure 9.39

Drain (bitline) current versus control gate (wordline) voltage transfer characteristics of the MOSFET in a flash cell: if the cell is programmed to a high V_T (logic "0"), and a read voltage is applied to the wordline that is below this V_T, the MOSFET does not conduct, and there is negligible bitline current. On the other hand, if the cell had been erased to a low V_T state (logic "1") the MOSFET is turned ON, and there is significant bitline current.

Macronix plans to heat up flash memory to keep it from burning out

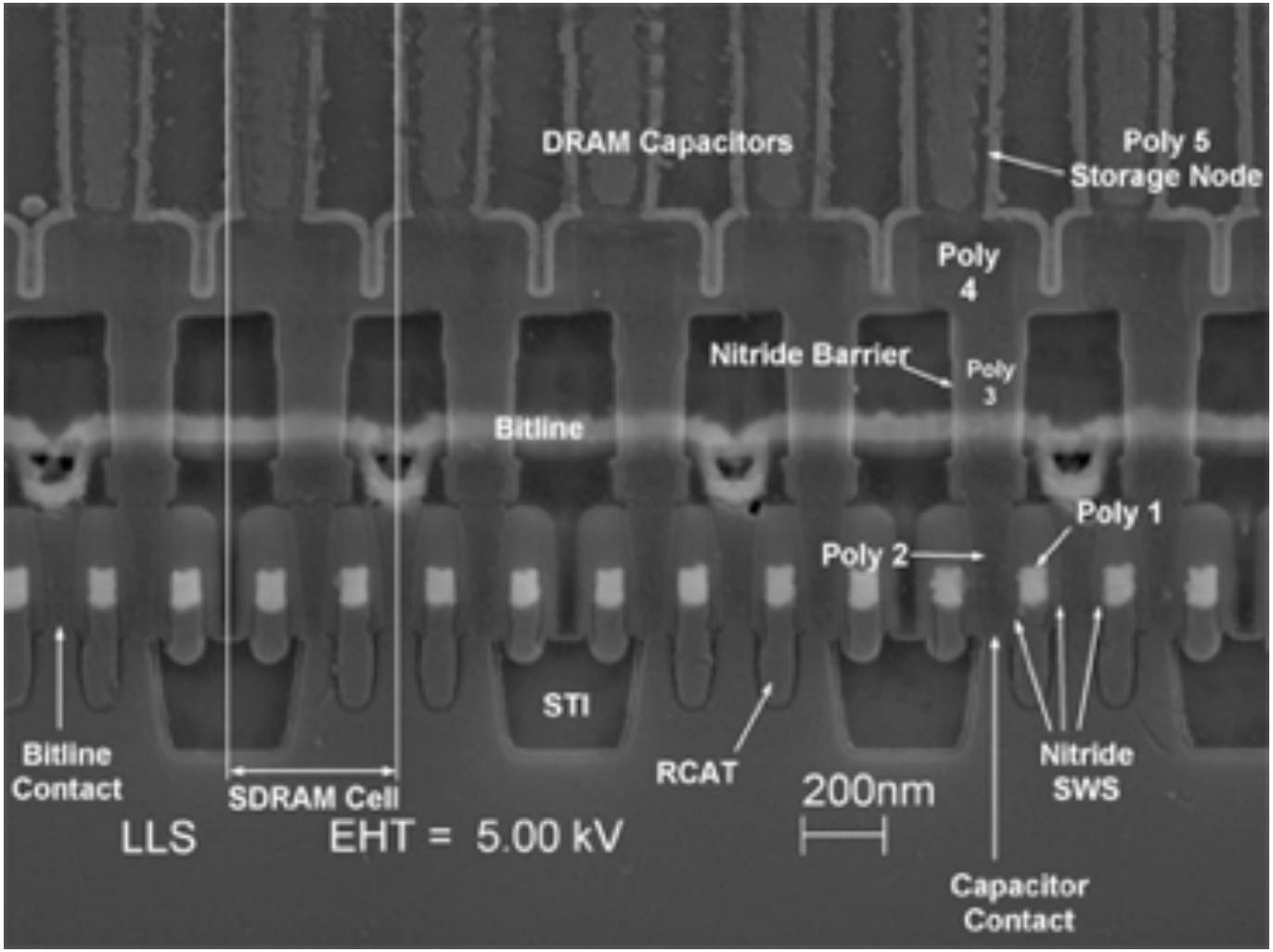
By **Sean Buckley** posted Dec 3rd, 2012 at 6:09 AM



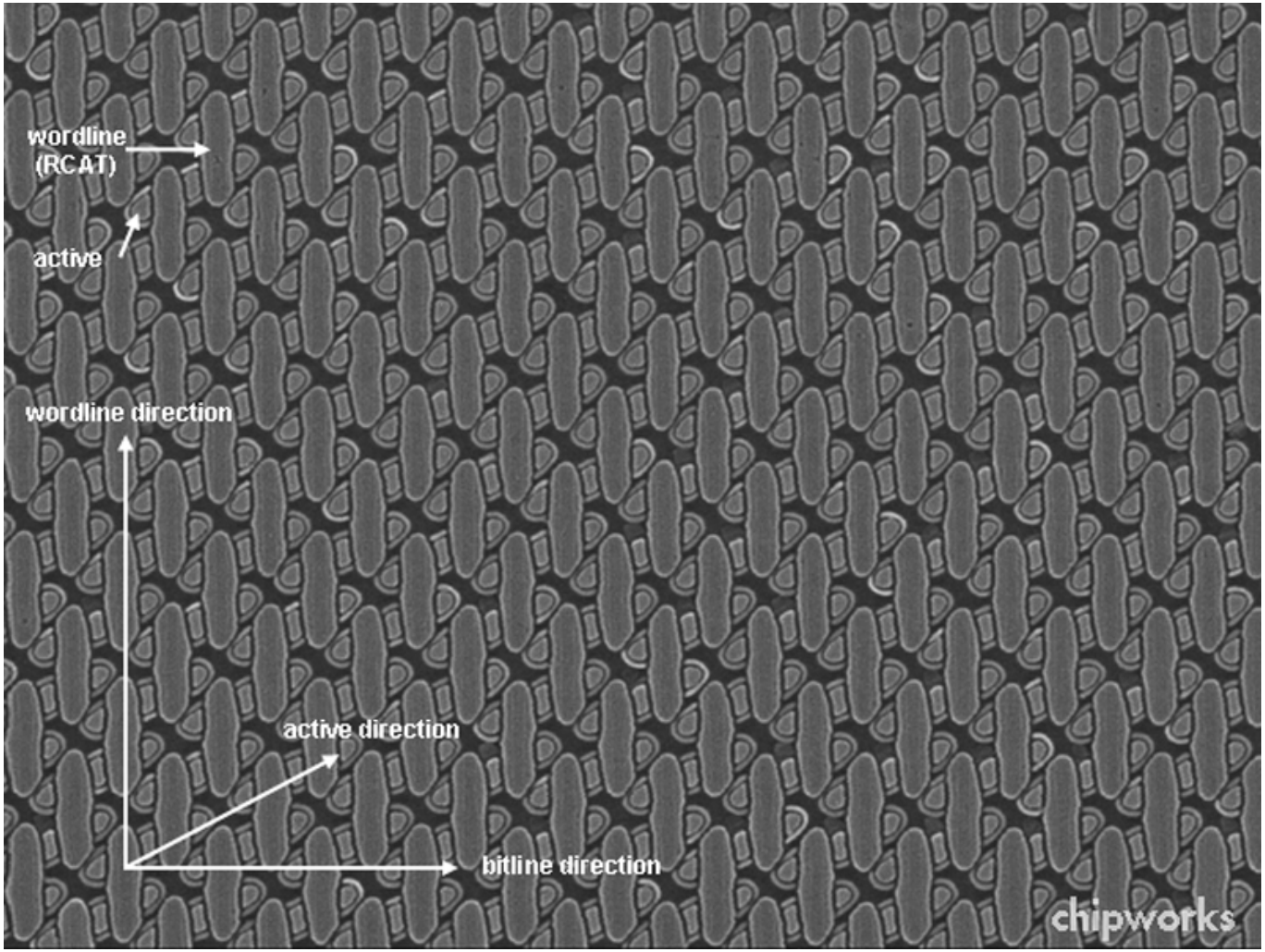
Despite the looming threat of being replaced by phase-change memory, contemporary memory modules aren't quite ready to be shown the door -- engineers at Macronix have found a way to revive spent NAND flash cells. Most flash modules fail after being written to and erased about 10,000 times, but Macronix found that the tired memory could be restored by baking it for extended periods of time. The team funneled the time consuming and cumbersome solution into a more practical package: a redesigned memory chip that packs onboard heaters. The new modules are designed to periodically heat focused groups of memory cells to 800 °C (1,472 °F) for a few milliseconds, effectively "healing" worn cells.

Researchers found that heated chips could tolerate more than 100 million write/erase cycles *and* erased faster at higher temperatures. The team said the power drain of the heaters shouldn't effect battery life, either -- chips don't have to be heated often, and when they do, it can be done while prospective devices are recharging. Macronix will be presenting the technology at the IEEE International Electron Devices Meeting next week, but project deputy director Hans-Ting Lue wouldn't say when the company plans on taking the technology to market. Lue *was* willing to speculate on what might become of it, however. "This may evolve into a 'thermally assisted' mode of operation that gives both better performance -- such as the faster erasing -- and better endurance flash memory." Faster, more reliable, super-heated memory. Sounds fine by us.

- DRAM cross-section view… why capacitors on top and not side-by-side with FETs?



- Samsung K4B1G0846F 48 nm 1 Gb DRAM
- 10^9 of these! Can any fail?



COMPONENTS memory, storage

Crossbar takes on DRAM and flash storage with super fast, super long-lasting RRAM tech

Agam Shah, IDG News Service
@agamsh

Aug 5, 2013 5:45 AM

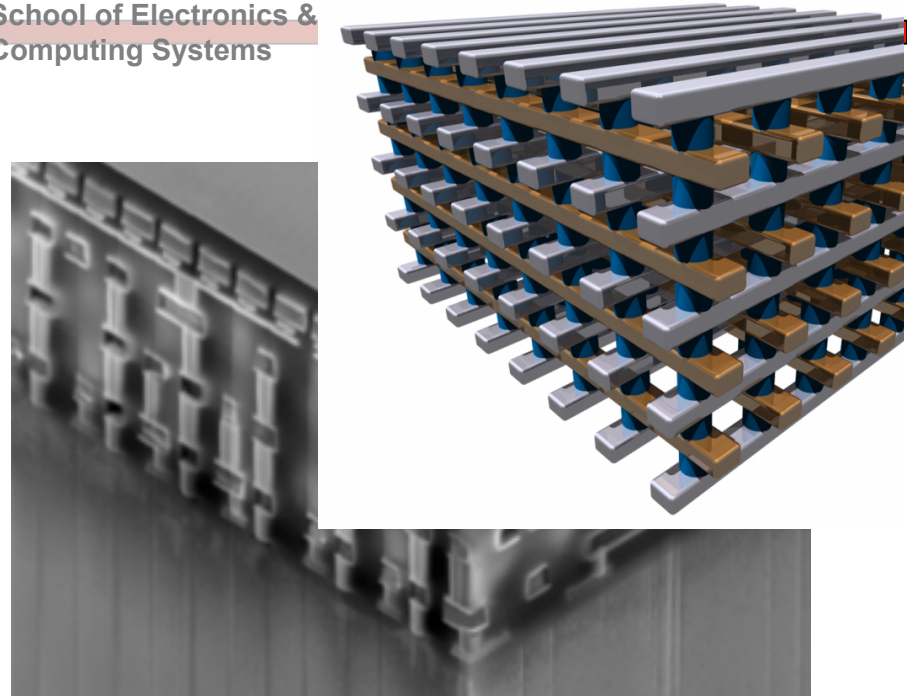
Startup Crossbar emerged from stealth mode Monday to announce its version of RRAM (resistive random-access memory), a new type of memory that could be a successor to flash storage and DRAM.

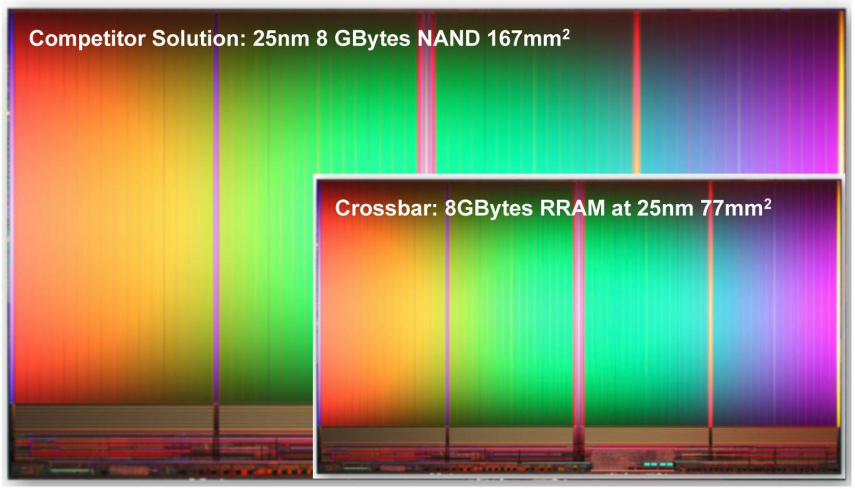
The company, founded in 2010, will make and license its RRAM, a nonvolatile memory, which will be smaller, faster and more power-efficient than NAND flash and RAM, said George Minassian, CEO of Crossbar.

"It is higher density ... and the current is much lower," Minassian said, adding that the memory's physical and power attributes make it a suitable replacement for storage in smartphones, tablets, PCs and servers.

Crossbar is claiming RRAM will deliver 20 times faster write performance, 20 times less power consumption and 10 times more durability than NAND flash. The memory chips will be stacked, and a 1TB module will be roughly half the size of a NAND flash module with similar storage, Minassian said.

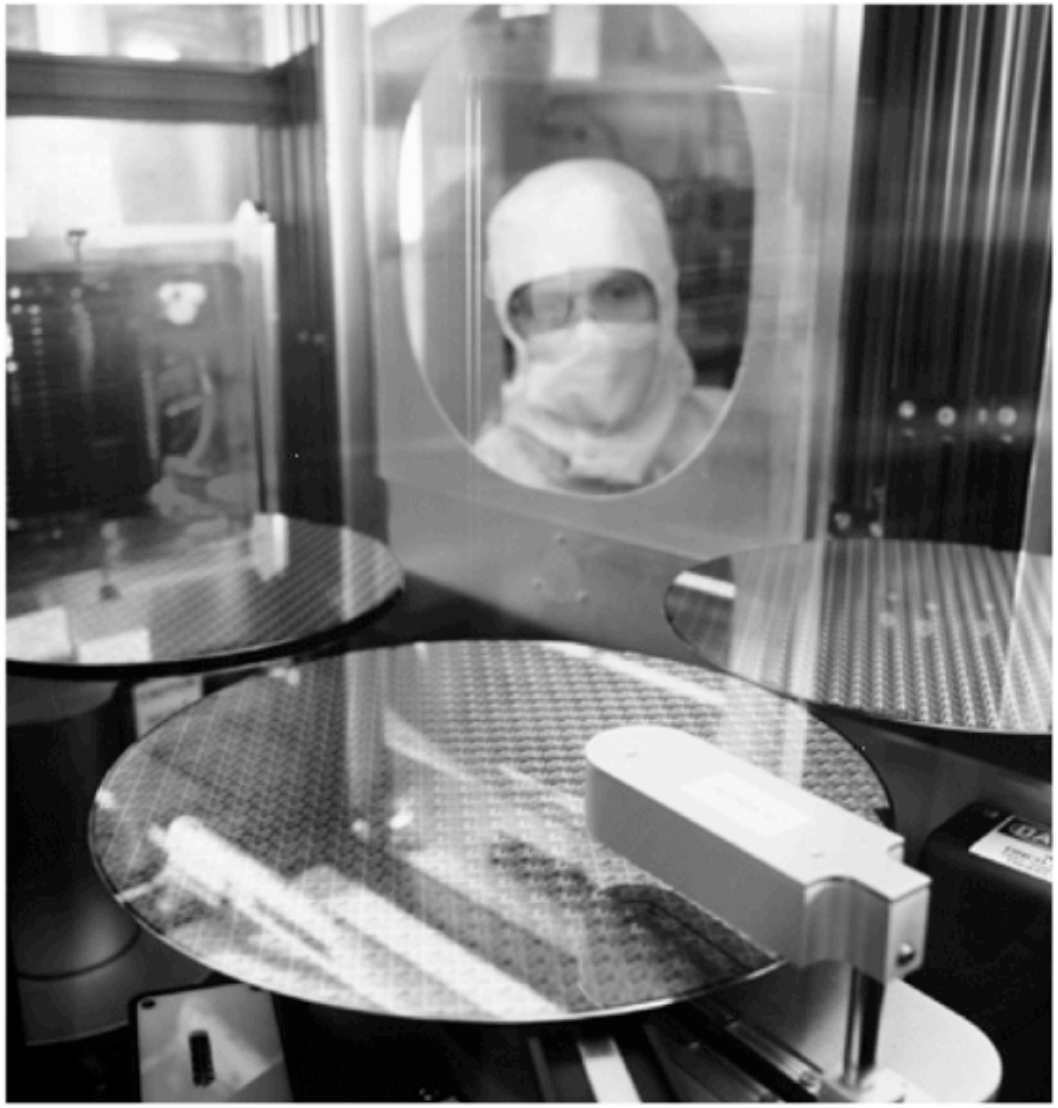
He could not estimate the price of a 1TB RRAM module, but said it will cheaper than NAND flash partly because RRAM is less expensive to manufacture.





Crossbar RRAM Technology
Half the Size of Traditional NAND

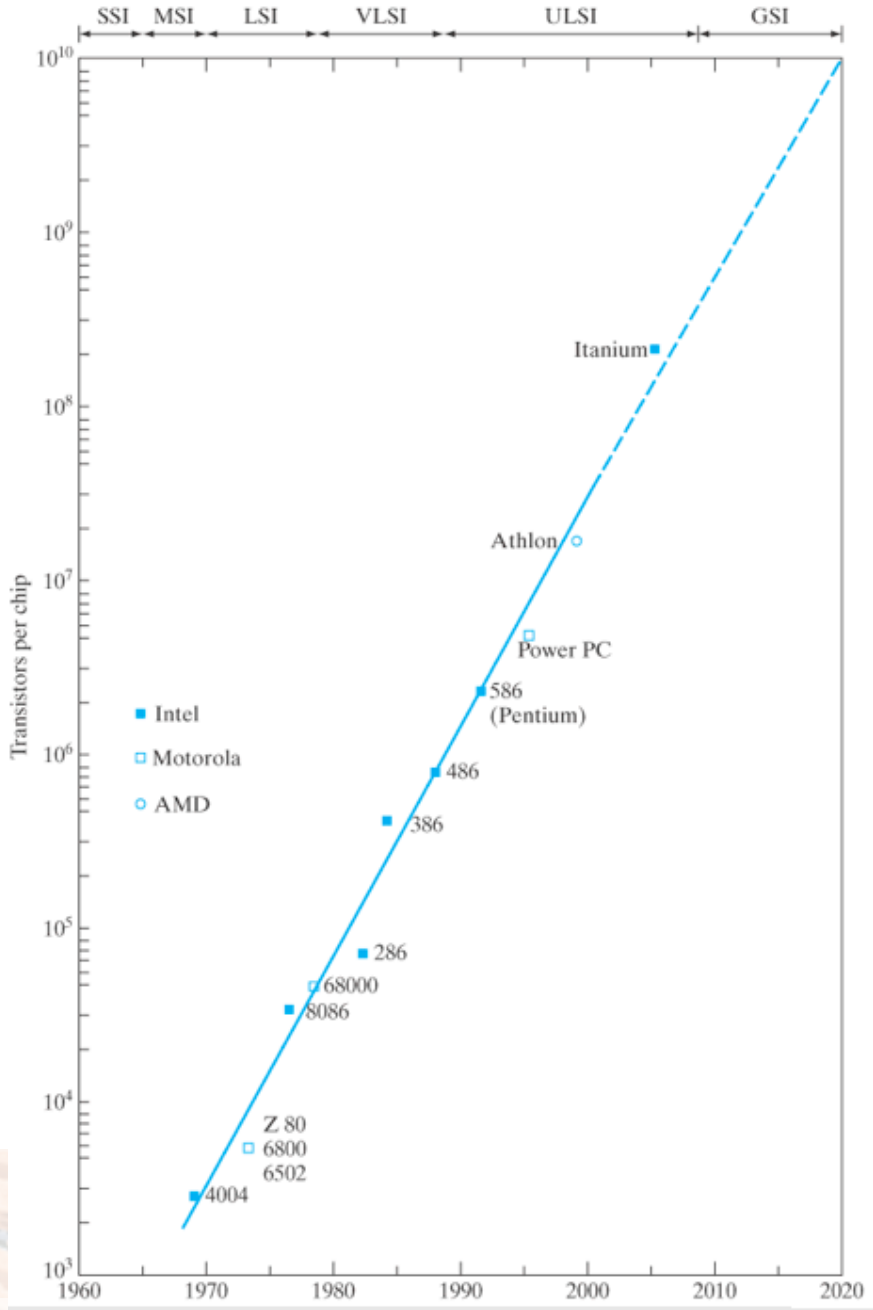
- Take a break! Make sure you are solid on the ☆'ed items!



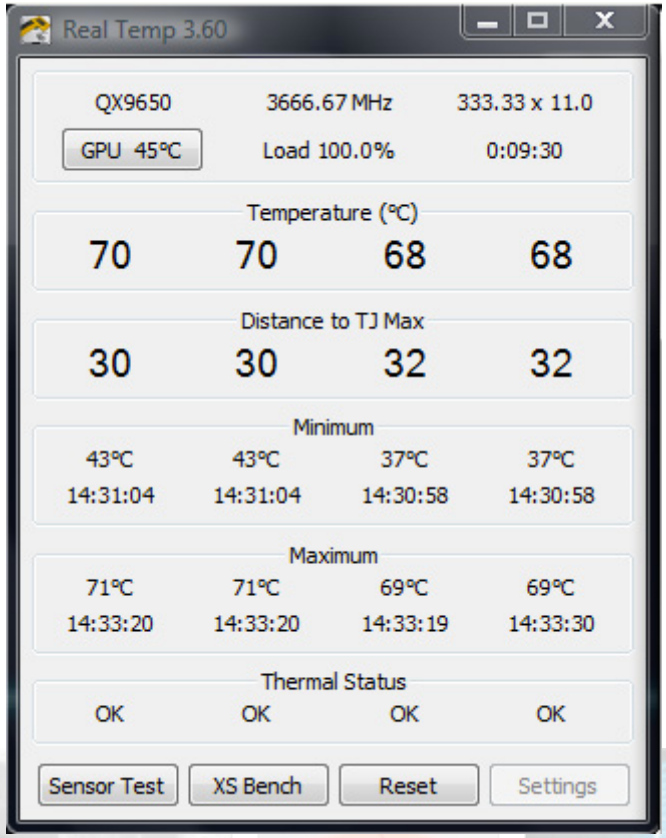
- 300 mm
Texas Inst.

- You are good at what you do (90% yield)?

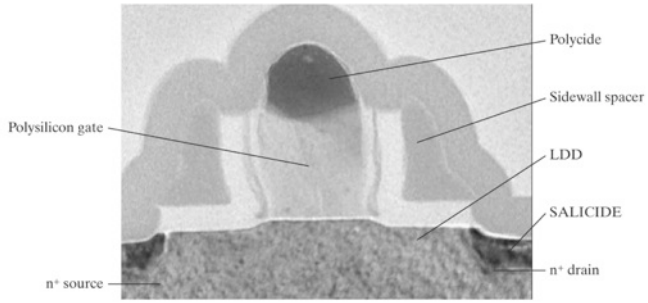
  pull out a calculator for 50 steps at this yield.

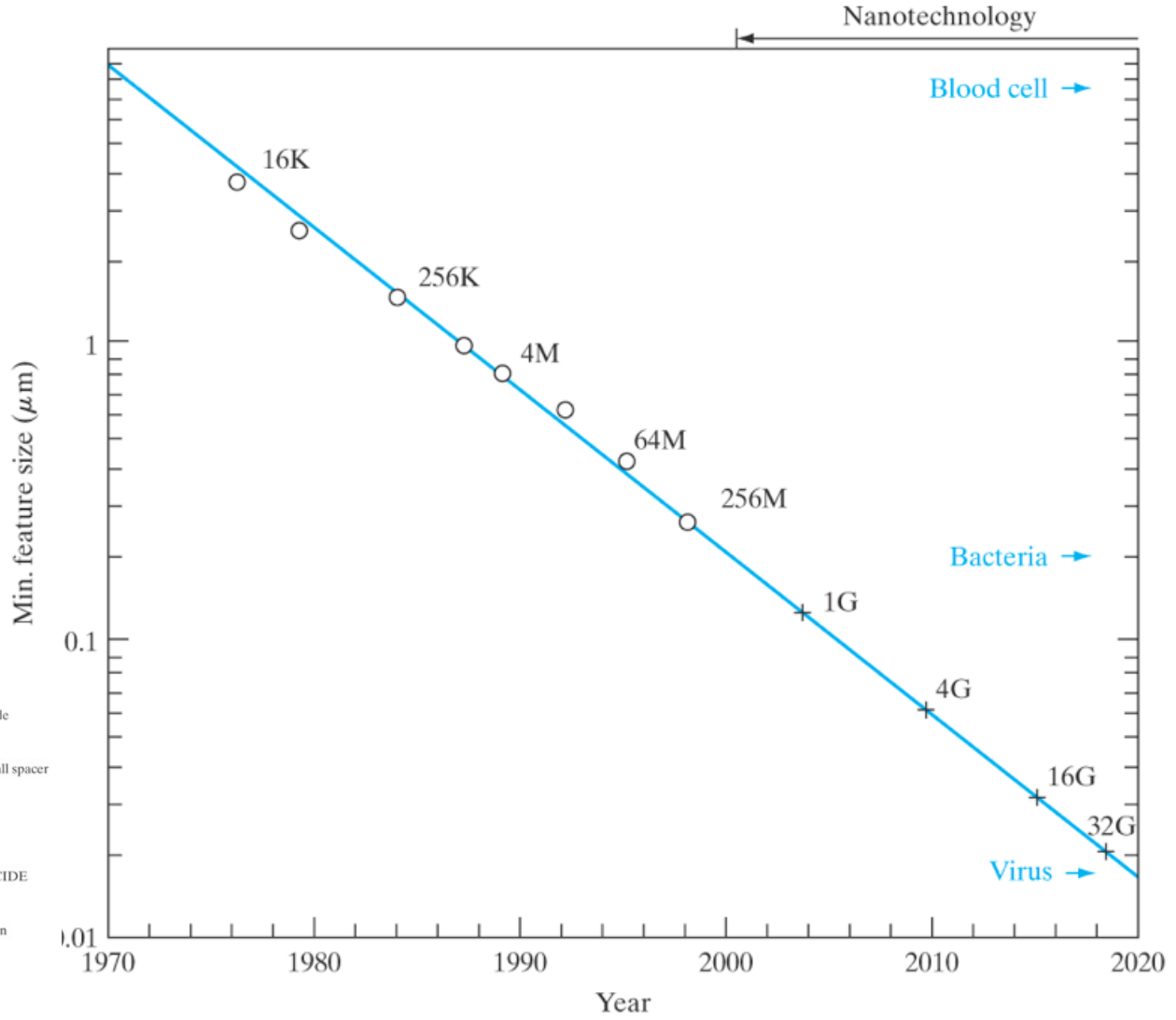


- Moores Law (transistors and cost)
- Has worked great for a long time, until this…. Why is processor core temp. a problem?

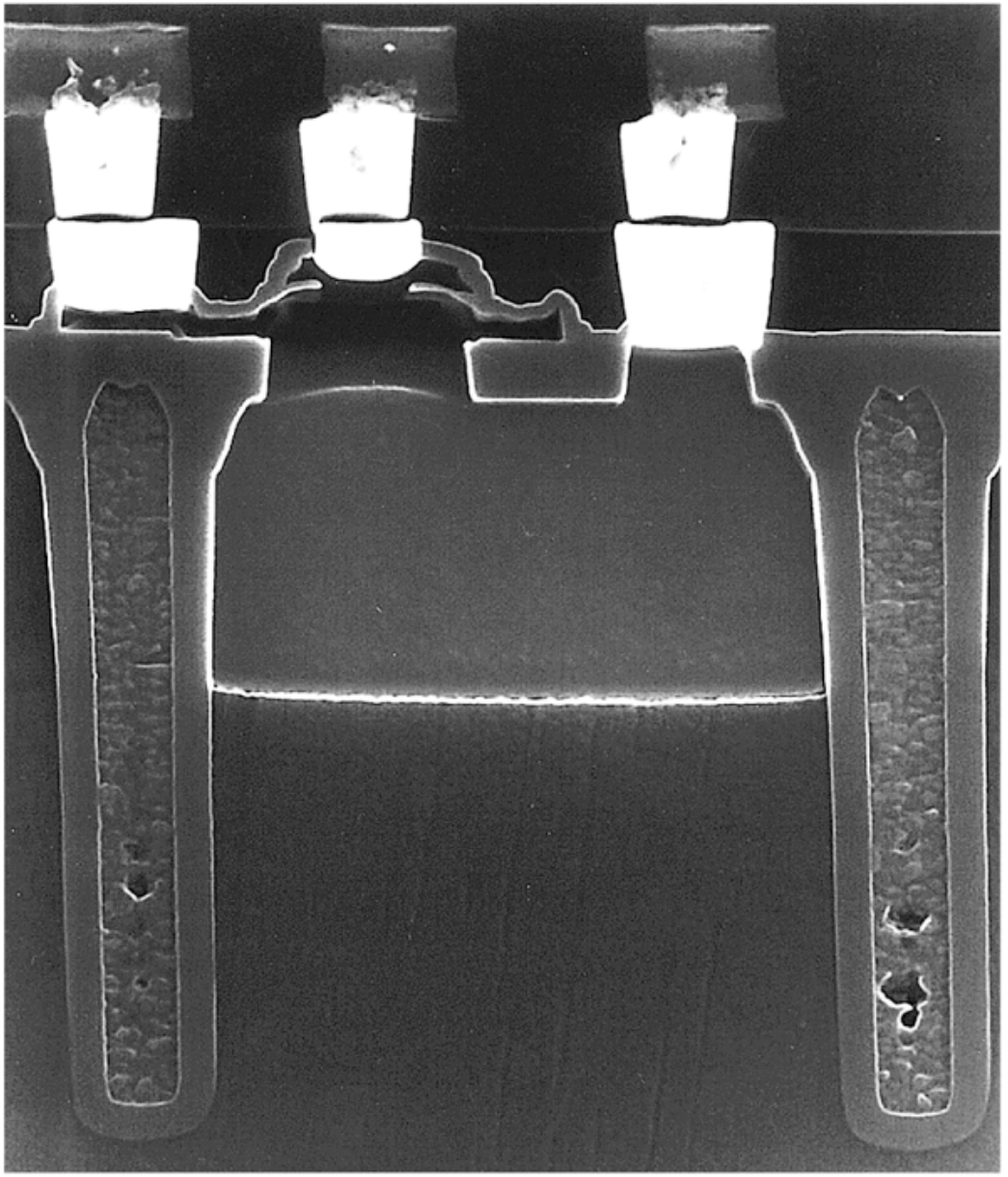


- Shorter source-to-drain (gate) = reduced R and C = faster and lower power devices!

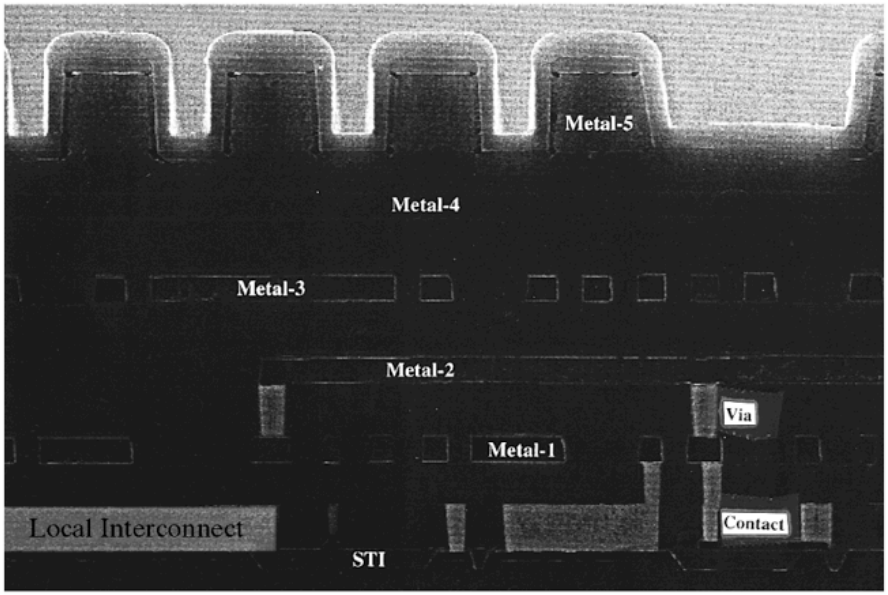


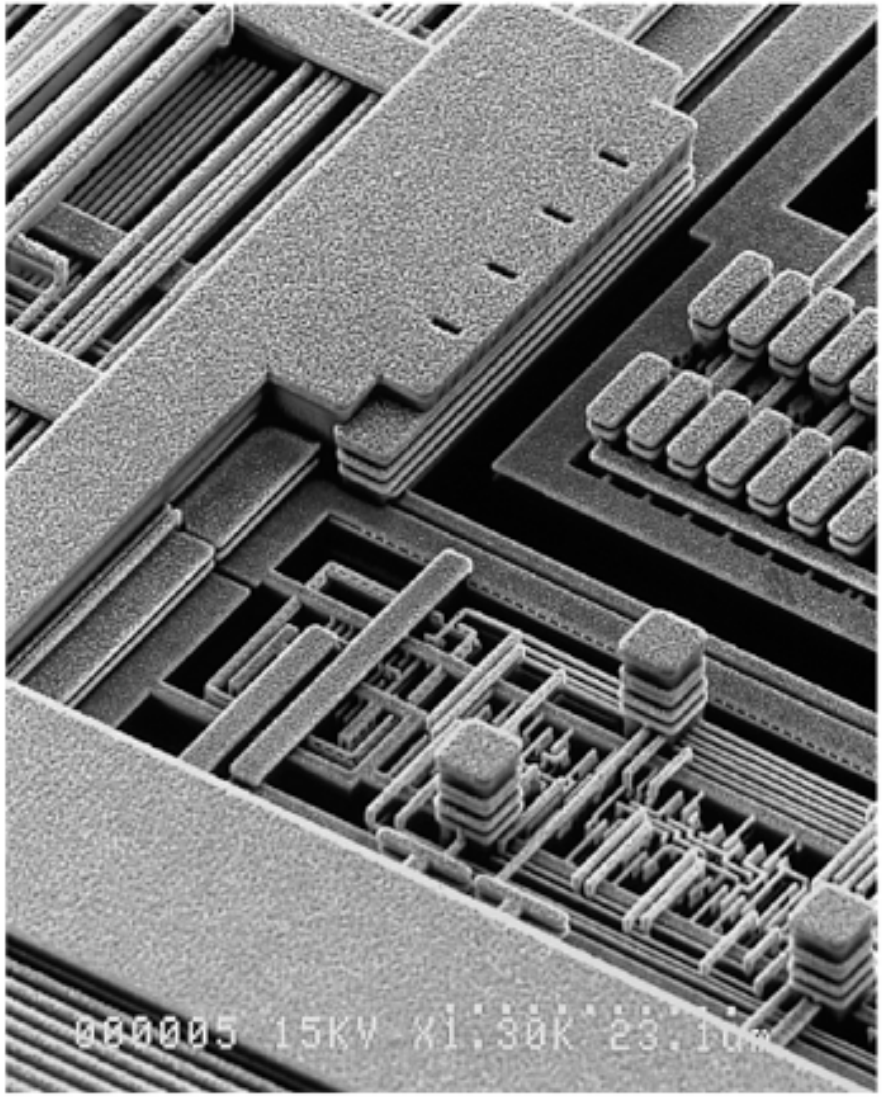


- Trench isolation (further isolate devices), even if reverse biased, junctions have capacitance (parasitic) and leakage currents…

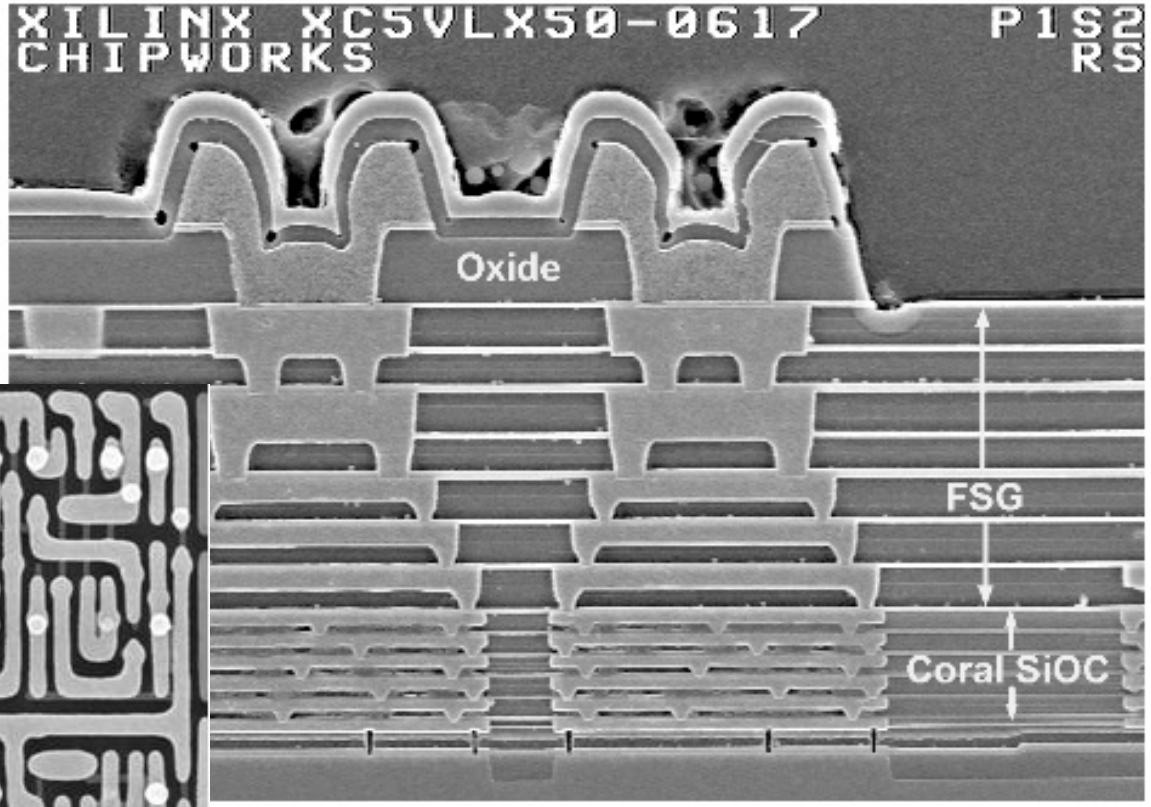


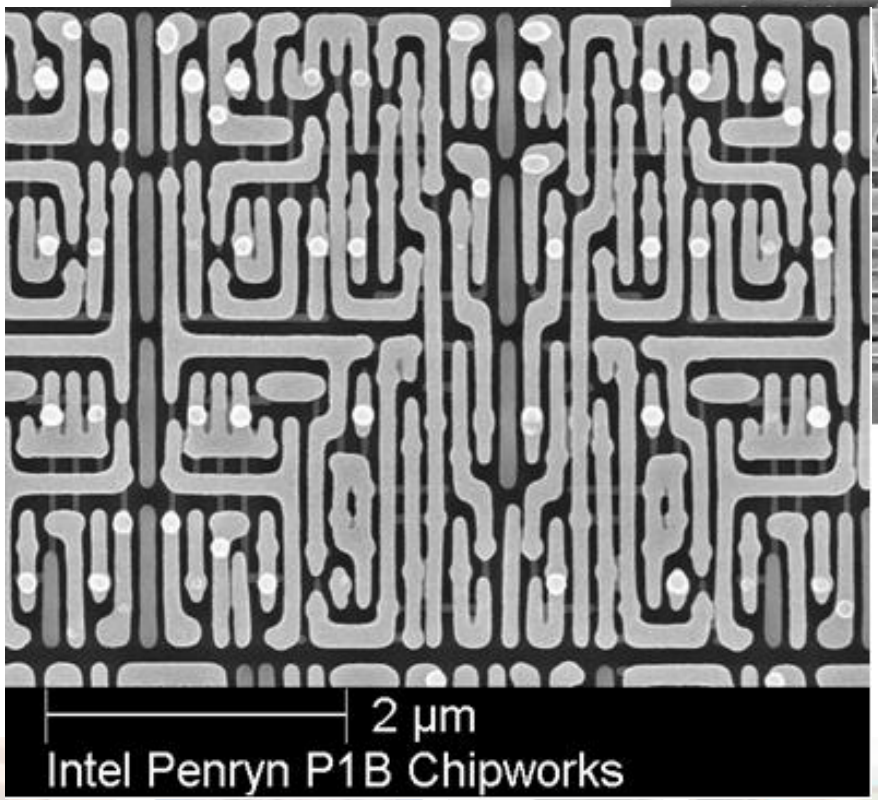
- Simply getting the ‘wiring’ right is a major challenge: minimize parasitic capacitance and resistance (RC time constant).
- Novel fluorinated materials ‘low k’ (ε_r~2)
- Now some are up to >12 layers…





- ~1B transistors on a chip, again, and >10 wiring layers on top of that… *Again, how many wire shorts can be tolerated?*





http://www.chipworks.com/en/technical-competitive-analysis/resources/technology-blog/2008/03/

Pressure Builds on Gate First High-k

Problems with the gate-first approach to high-k/metal gate deposition may force IBM to switch to the gate-last approach pioneered by Intel, technologists said this week at the International Electron Devices Meeting (IEDM) in Baltimore. GlobalFoundries and other members of the Fishkill Alliance are putting pressure on IBM to reconsider its gate-first approach, which technologists said has problems with yields, threshold voltage stability, and mobilities.

David Lammers, News Editor -- Semiconductor International, 12/9/2009

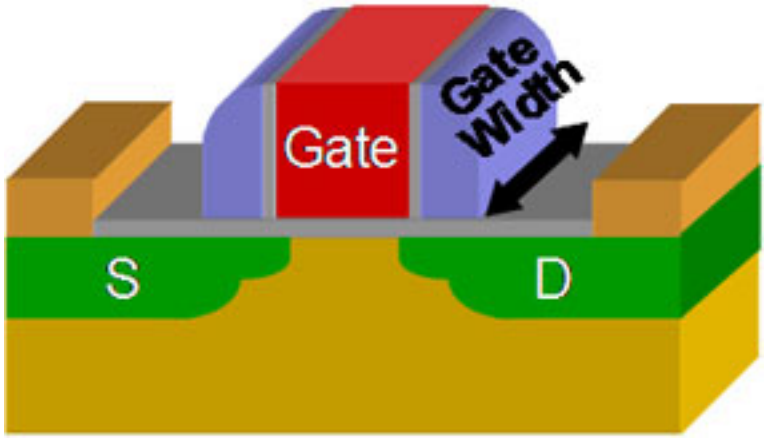
Asked about a switch to a gate-last approach at the 22 nm node, Khare said, "I am surprised at that kind of talk. Every technology has challenges, which is why we continue to work at it and develop solutions. We take it one node at a time." He added, "At this point, no one knows what will happen at the 15 nm node. It could be finFETs that come in by that time." The fully depleted, extremely thin SOI (FD-ETSOI) approach that IBM is pursuing would provide greater electrostatic control, and take some of the burden off of the oxide layer.

- From: *Novel Devices to Overcome Planar Limits and Enable Novel Circuits*, Leo Matthews, Freescale Semiconductor

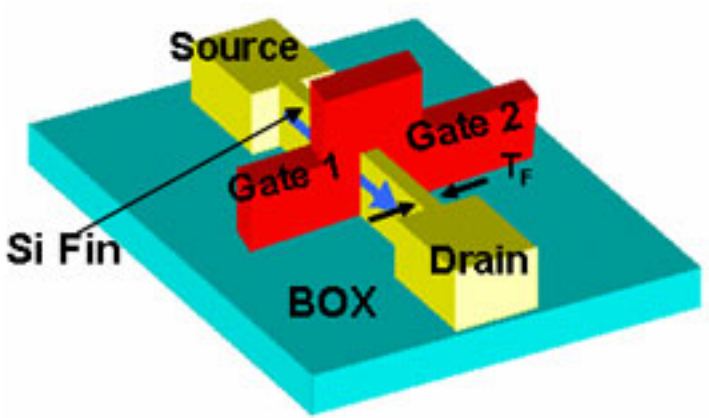
(1) Traditional scaling (channel length, T_{ox}) of planar MOSFETs is rapidly encountering significant obstacles to meeting performance targets within acceptable power limits.

(2) Double-gated MOSFETs (FinFETs) can change the scaling paradigm and allow continued performance improvements within acceptable power limits. *Channel width is vertical, why is that better? What else looks better about this?*

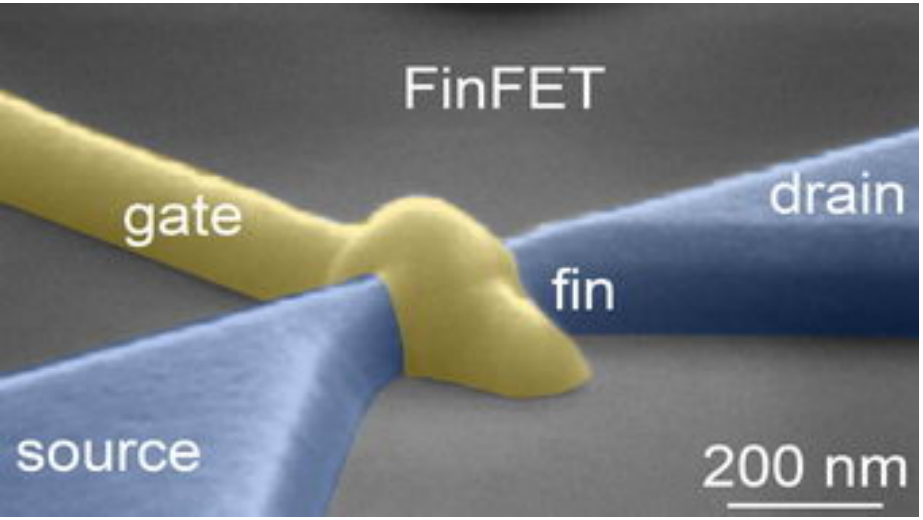
Planar Bulk FET

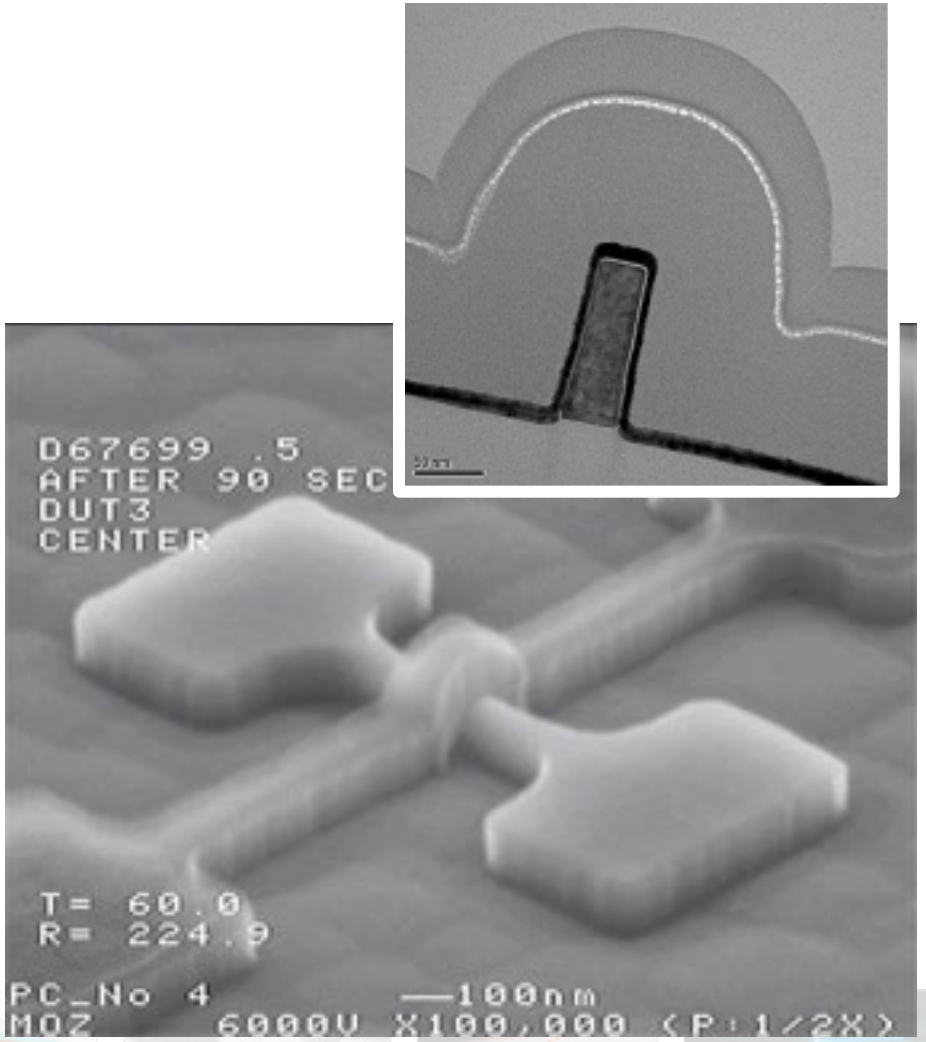


Double Gated FinFET

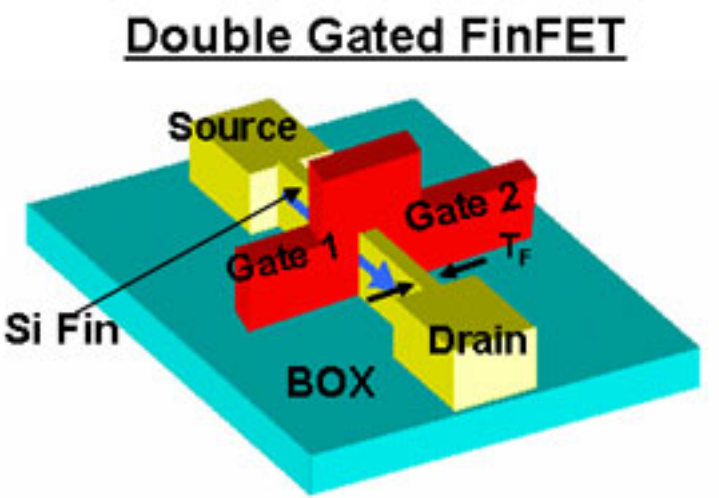


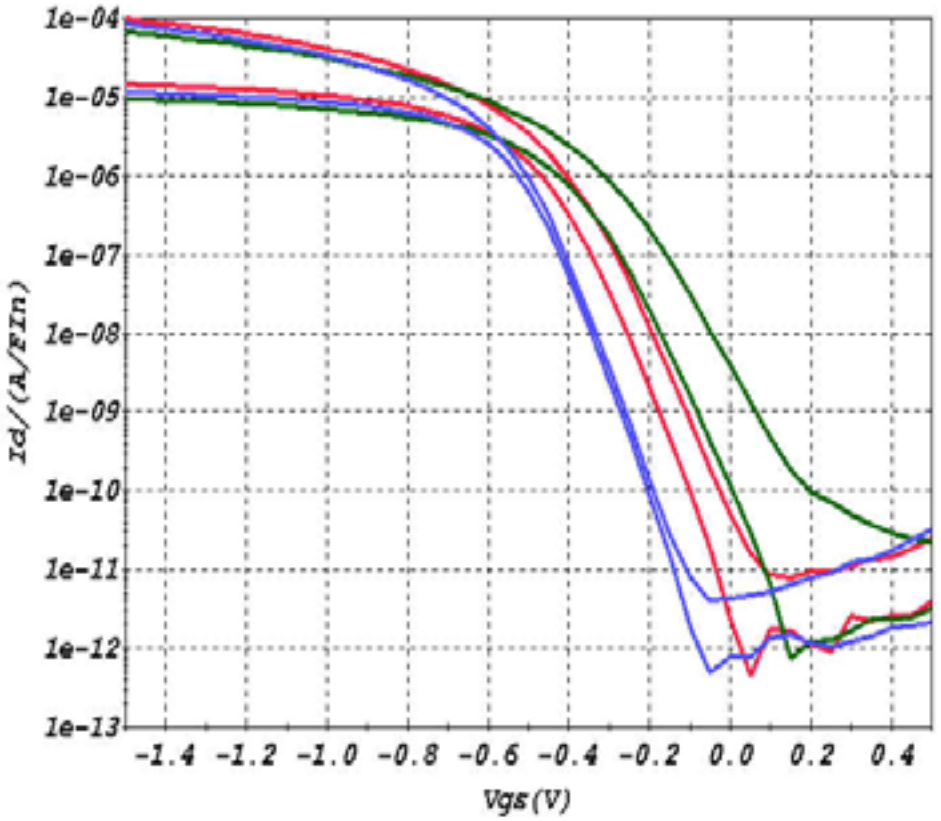
- From: *Novel Devices to Overcome Planar Limits and Enable Novel Circuits*, Leo Matthews, Freescale Semiconductor



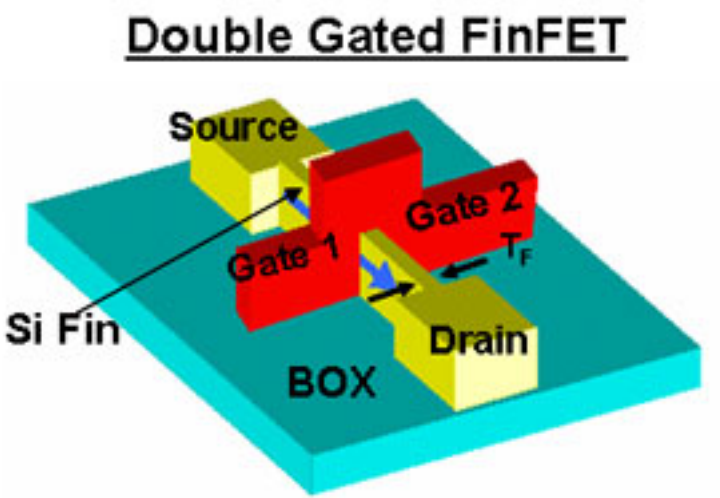


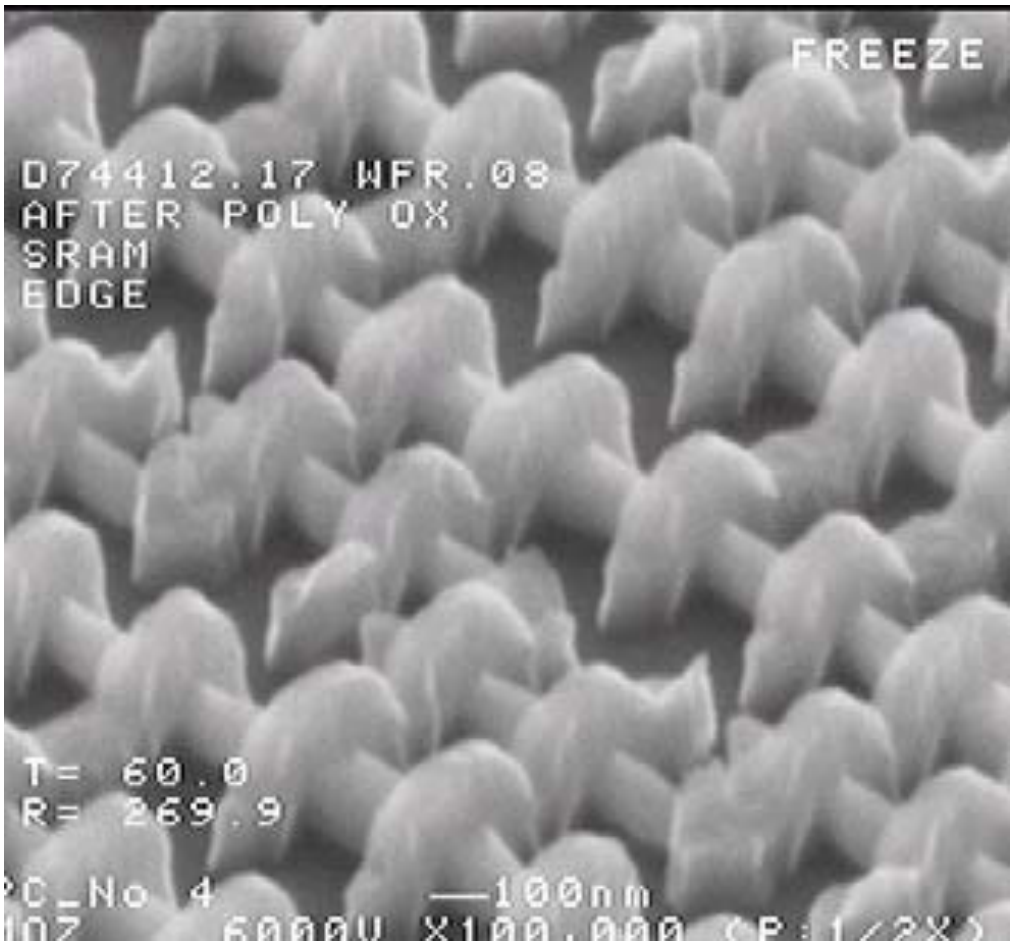
- From: *Novel Devices to Overcome Planar Limits and Enable Novel Circuits*, Leo Matthews, Freescale Semiconductor





- From: *Novel Devices to Overcome Planar Limits and Enable Novel Circuits*, Leo Matthews, Freescale Semiconductor





An array of FinFET SRAM cells patterned over 100 nm topography

Globalfoundries Challenges Intel in 14nm Chip Manufacturing

By Jeffrey Burt | Posted 2012-09-20 Email Print

Globalfoundries is speeding up the timeline for its 14nm process that will feature 3D transistors, looking to match Intel in both timing and architecture.

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Globalfoundries is making an aggressive move to challenge Intel in chip manufacturing, with officials announcing that the company will be ready by 2014 with a 14-nanometer process that will include a three-dimensional transistor architecture similar to Intel's Tri-Gate method.

Globalfoundries' 14nm-XM (eXtreme Mobility) process will include a 3D FinFET transistor technology that will enable higher performance and greater power efficiency in mobile devices like smartphones. It also will come only a year after the foundry begins offering its 20nm process. If Globalfoundries can hit its target of 2014 for the 14nm-XM, it will leapfrog over other foundries like Tawain Semiconductor Manufacturing Co. (TSMC) and dovetail with Intel's plans to roll out its 14nm chips that same year.

The foundry's 14nm-XM architecture will include a combination of a 14nm FinFET device and Globalfoundries' 20nm low-power processes. Bringing together parts of varying size to create a new chip might seem odd, but it makes sense, according to Roger Kay, principal analyst at Endpoint Technologies Associates.

Endpoint Technologies' Kay said Globalfoundries had several advantages in being able to fast-track its development of the 14nm-XM process, including 10 years of work on the 3D transistor architecture that IBM undertook and gave to the Common Platform, a chip design group that includes Globalfoundries, IBM and Samsung Electronics. One benefit is being able to leverage the capabilities of high-K metal gate (HKMG) technology, which cuts down on the amount of electrical leakage as chips get smaller.

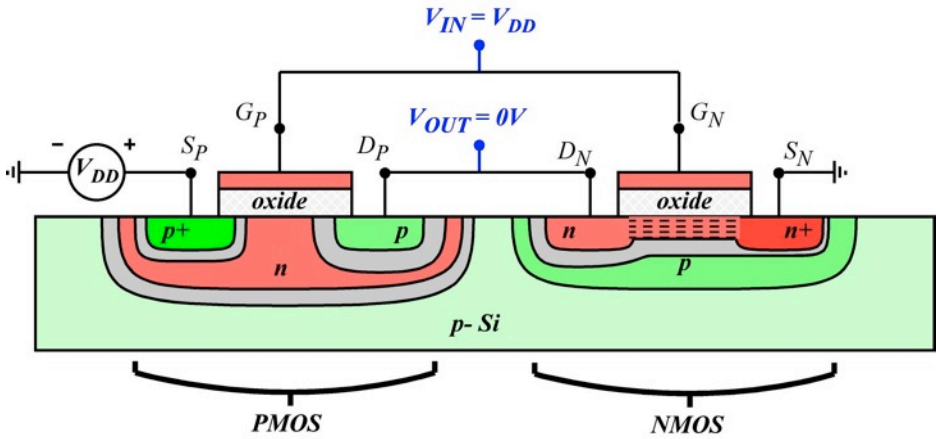
"It was critical to master this technique, which Intel has had since 2007," Kay said. "It was only in 2010 that AMD was able to get HKMG up and running in its 32nm processors, which have both processing and graphics on the same piece of silicon."

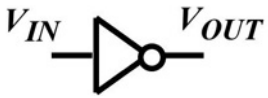
Development of the 14nm-XM technology already has begun in Globalfoundries' new Fab 8 in Saratoga County, N.Y., and the foundry is making early process design kits (PDKs) available now. Tape-outs by customers of the new SoCs are expected to happen next year, according to officials.

While Globalfoundries' 14nm-XM technology will come out the same time as Intel's 14nm chips, the fact that they are SoCs aimed at mobile devices like tablets and smartphones plays to Globalfoundries' strengths, Endpoint Technologies' Kay said. Intel dominates the PC and server chip markets, but it still is trying to get some traction in mobile devices. Meanwhile, Globalfoundries, TSMC, ARM and others already have strong positions in the mobile device space.

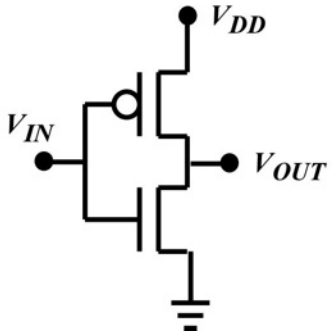
"Globalfoundries has come from way behind to nip at Intel's heels," Kay wrote. "The 14XM will hit the market in volume in mid-2014, right on top of Intel's 14nm processors. And Globalfoundries and its customers have the pole position in high mobility, offering an ultra-low power mobile SoC with a whole ecosystem around it rather than just a processor. â¦ A race that had almost gotten boring is suddenly exciting again."

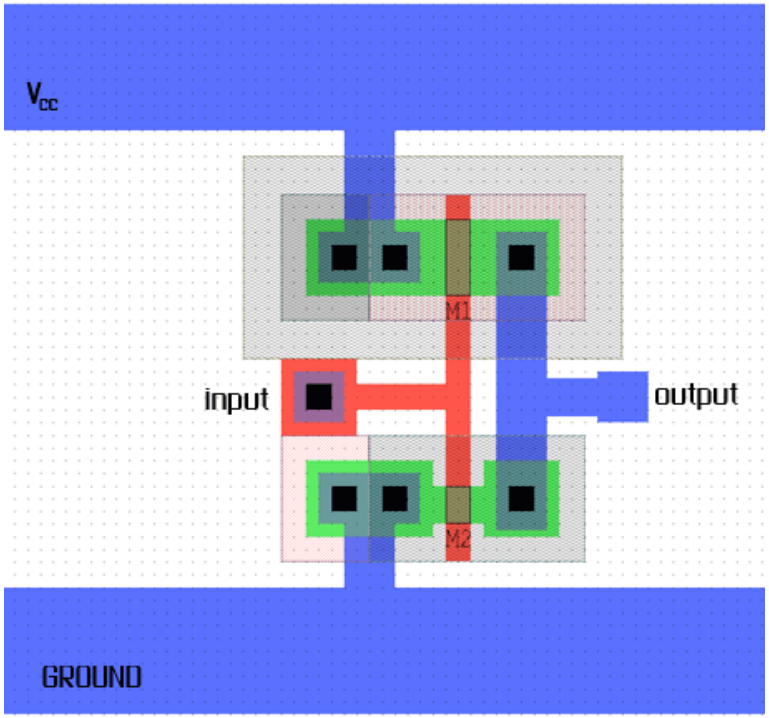
- This is an inverter…. can you figure out all the layers?





V_{IN}	V_{OUT}
0V	5V
5V	0V

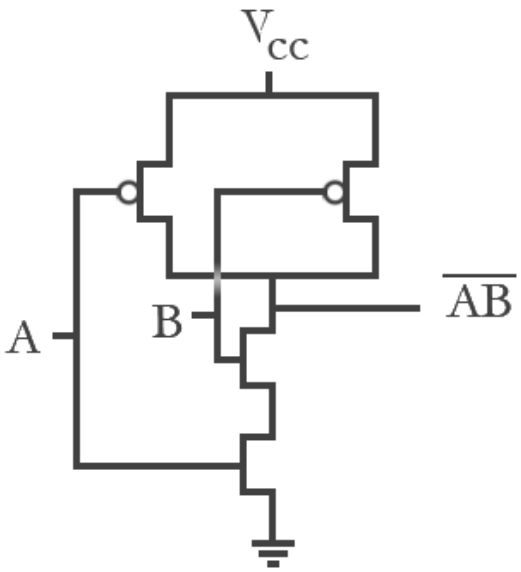


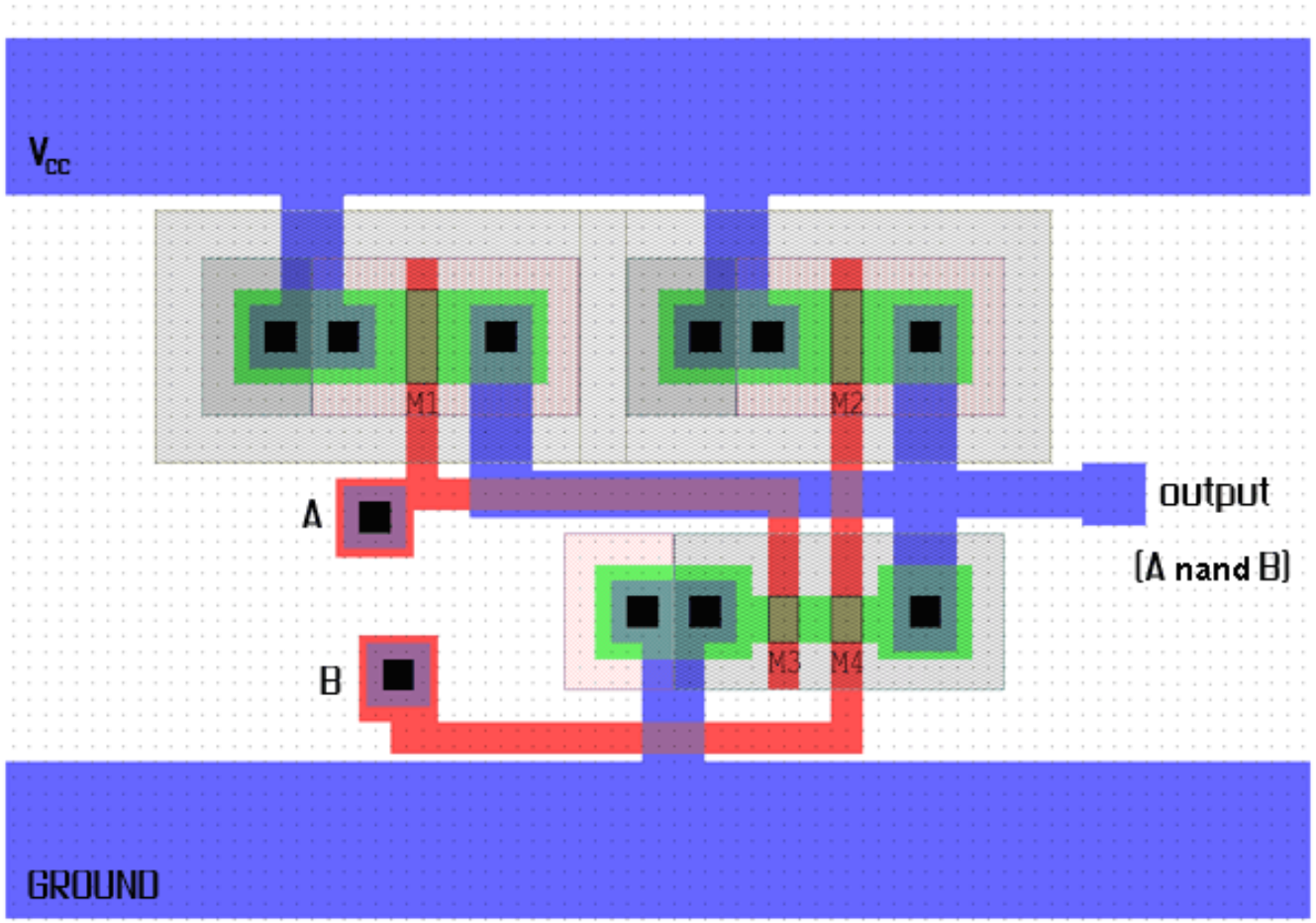


www.sccs.swarthmore.edu/users/06/adem/engin/e77vlsi/lab3/

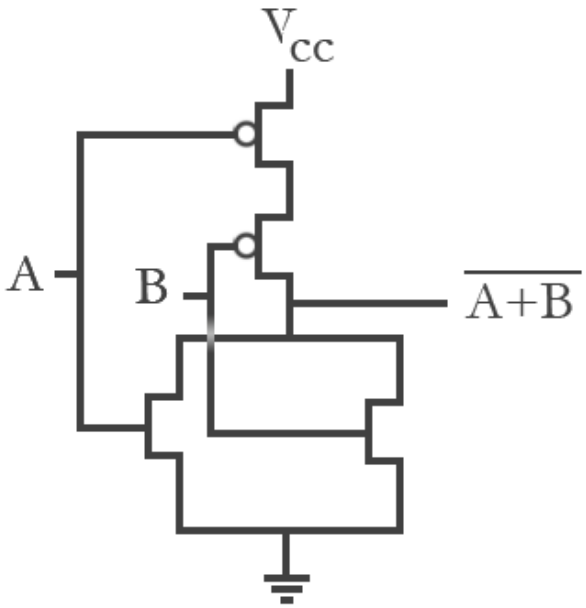
Funny, I randomly picked my colors for materials when starting this course and they seem to match up!

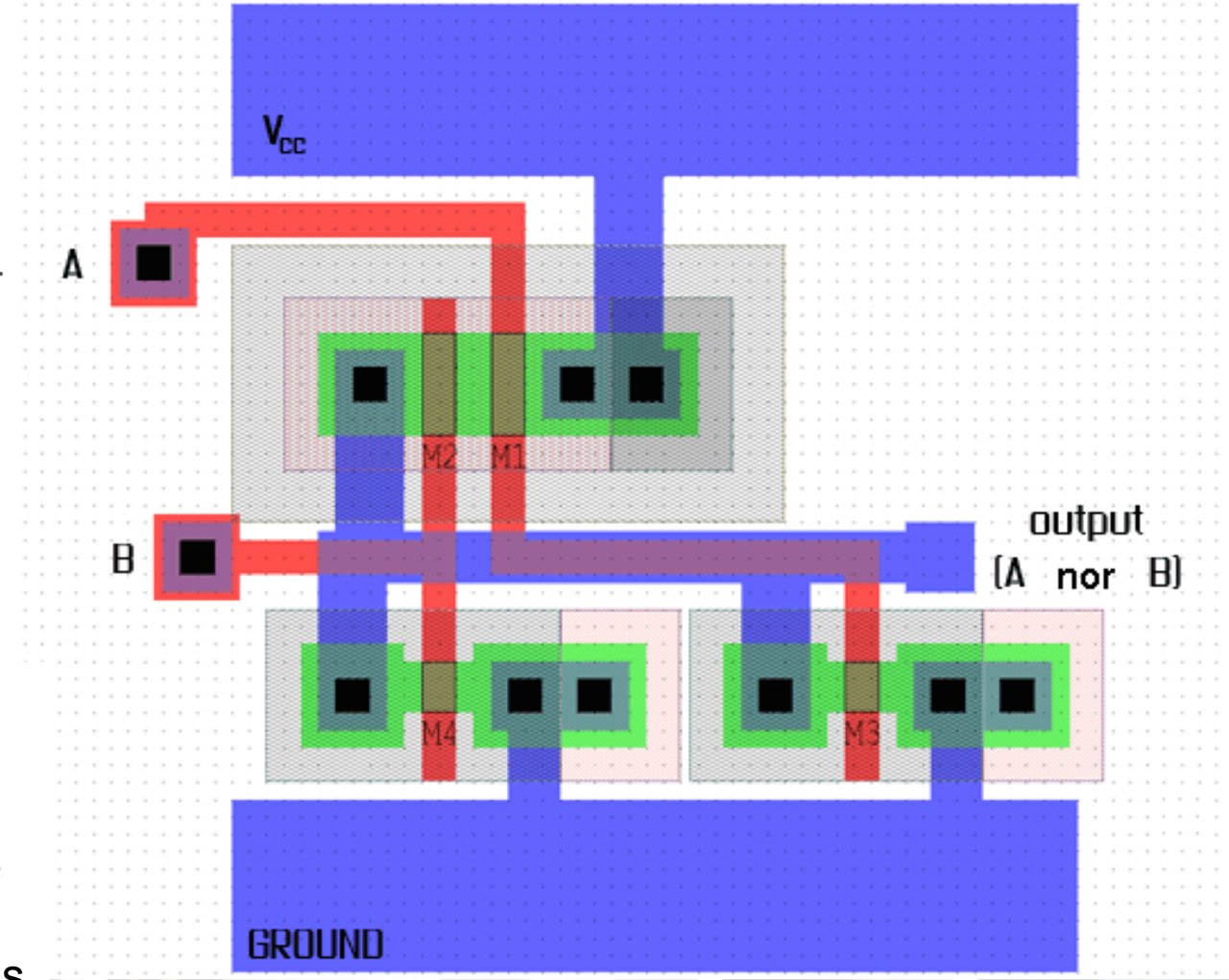
- NAND (courtesy : www.sccs.swarthmore.edu/users/06/adem/engin/e77vlsi/lab3/





- NOR (courtesy : www.sccs.swarthmore.edu/users/06/adem/engin/e77vlsi/lab3/

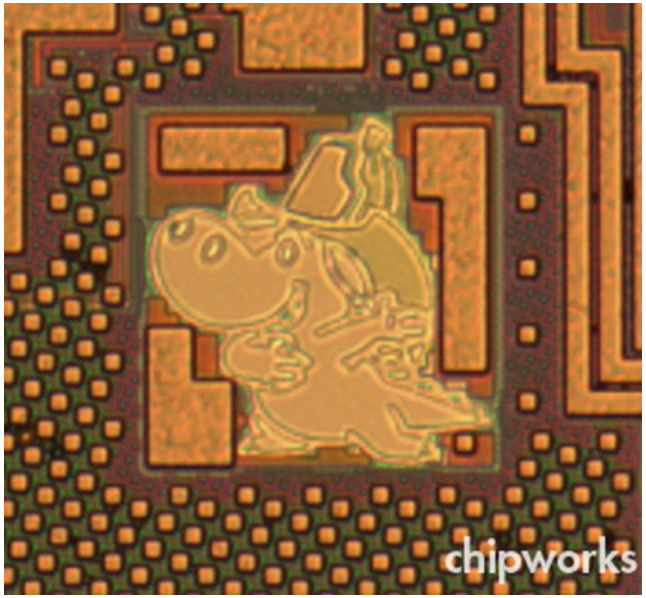


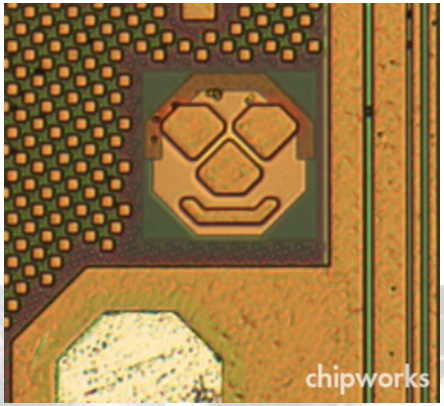


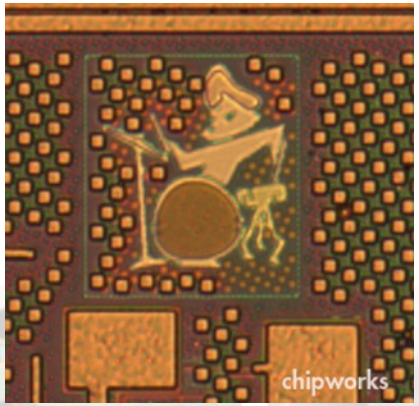
- Are these SSI, MSI, LSI, VLSI, ULSI?

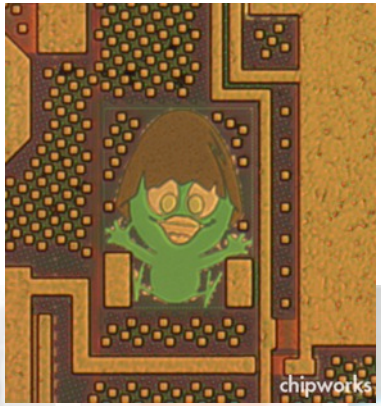
- With VLSI, how might the design approach change? Think packaging and various levels of team roles…

- From: www.chipworks.com/en/technical-competitive-analysis/resources/technology-blog/2011/02/









- That is all for MOSFETS! Make sure you are solid on the ☆'ed items!

How to Get 5 Gbps Out of a Samsung Graphics DRAM

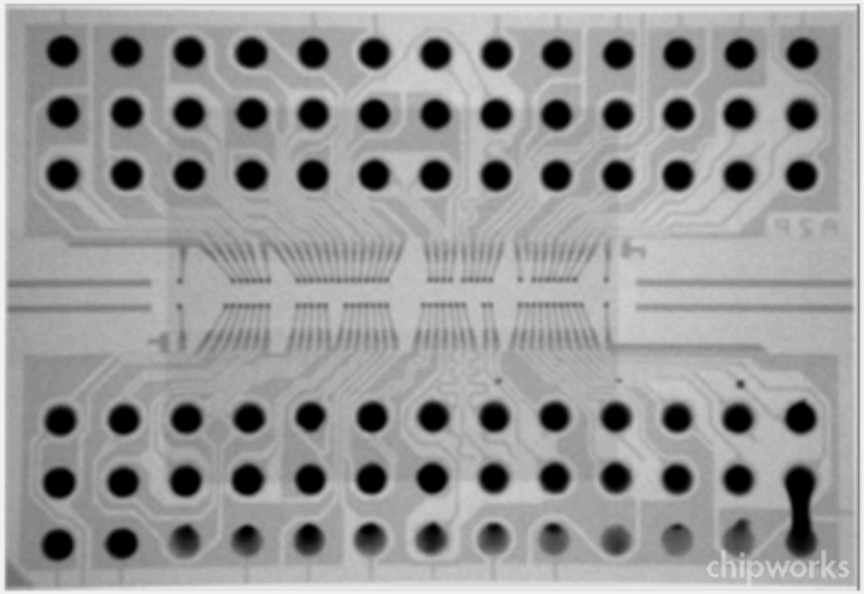
Monday, December 20th, 2010 *by Dick James*

It's well known that electronics games buffs like their image creation as realistic (or at least as cinema-like) as possible, which in image-processing terms means handling more and more fine-grained pixel data as fast as possible. That means more and more stream processors and texture units in the graphics processor to handle parallel data streams, and faster and faster memory to funnel the data in and out of the GPU.

We recently pulled apart a Sapphire Radeon HD5750 graphics board, containing an AMD/ATI GPU, running at 700 MHz, and supported by eight Gb (1 GB) of Samsung GDDR5 memory. This card is a budget card, but the ATI chip still boasts 1.04 billion transistors, 720 stream processors and 36 texture units, can compute at ~1 TFLOPS with a pixel fill rate of 11 Gpixel/s, and can run memory at 1150 MHz with 74 GB/sec of memory bandwidth. I'm not a gamer, but those numbers are impressive to me!

When we started looking at the memory chips, and decoded the part number, we found that we had Samsung's fastest graphics memory part, claimed to run at 5 Gbps. Graphics DRAMs are designed to run faster anyway, but 5 Gbps is three times faster than the fastest regular DDR3 (Double-Data Rate, 3rd Generation) SDRAM, which can do 1.6 Gbps.

So what makes this one so blazing fast? Beginning with the x-ray, the difference between a Graphics DDR5 when compared with a 1Gb DDR3 (K4B1G0846F-HCF8) part starts to show up. If we look at an x-ray of the DDR3 chip, we can see that it has the conventional wire-bonding down the central spine:



Plan-View X-ray of Samsung 1 Gb DDR3 SDRAM